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32

SH7211 CPU Board

M3A-HS11

User's Manual

Renesas 32-Bit RISC Microcomputers
SuperH™ RISCengine Family / SH7211 Group

User's Manual

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M3A-HS11 SCHEMATICS

Chapter1
Overview

1.1 Overview

The M3A-HS11 is the CPU board designed for users to evaluate the functionality and performance of the SH7211 group of Renesas Technology original microcomputers, as well as develop and evaluate the application software for this group of microcomputers. The SH7211's data bus, address bus and various internal peripheral circuit function pins are connected to the extension connector of the M3A-HS11, allowing users to evaluate the timing relationship with peripheral devices using measurement instruments or develop extension boards tailored to suit development purposes. Furthermore, the E10A-USB or the on-chip emulator made by Renesas Technology can also be connected to the M3A-HS11.

1.2 Configuration

Figure1.2.1 shows an example of system configuration using the M3A-HS11.

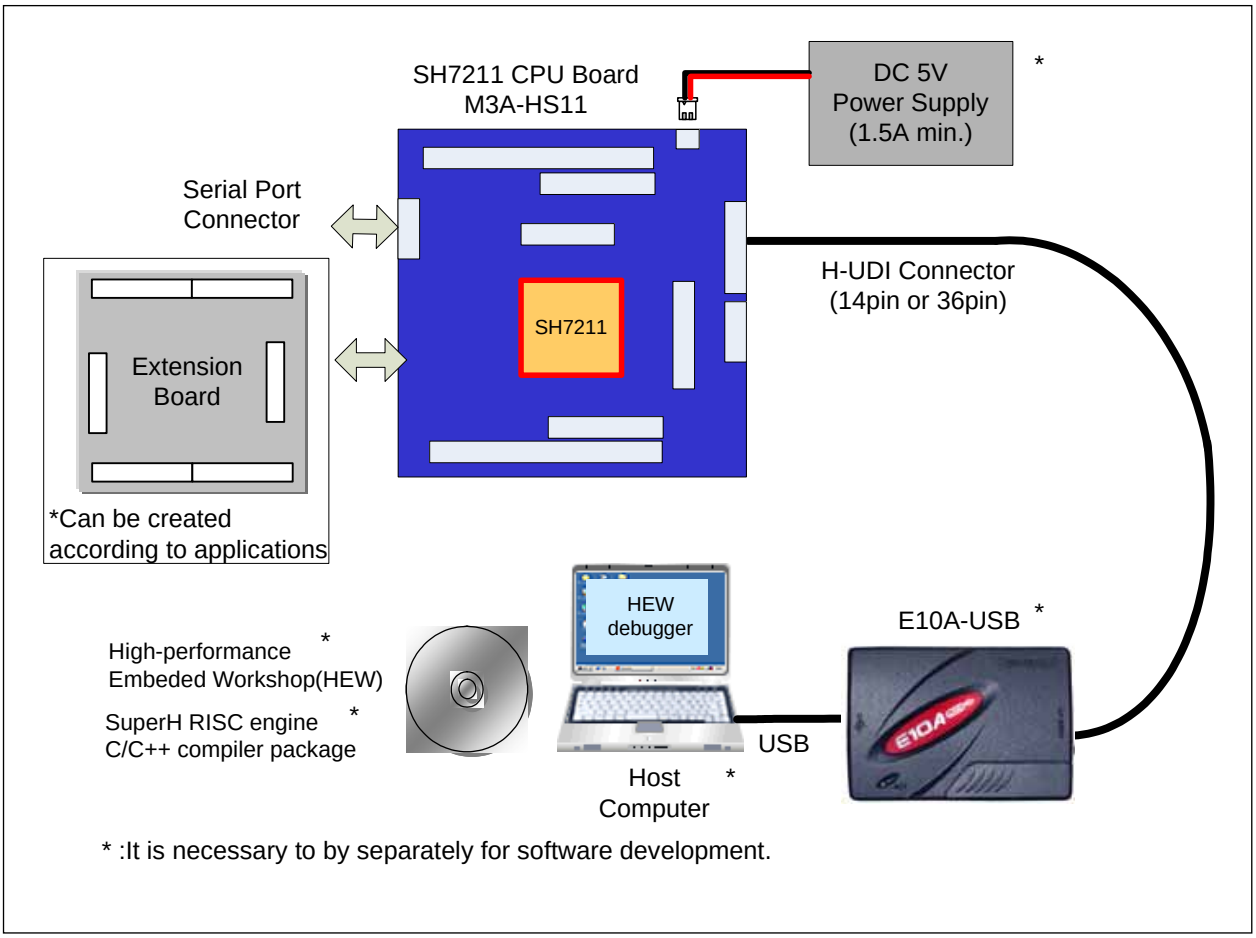


Figure1.2.1 Example System Configuration of M3A-HS11

1.3 External Specifications

Table1.3.1 lists external specifications of M3A-HS11.

Table1.3.1 External Specifications of M3A-HS11

No.	Item	Content
1	CPU	SH7211 ● Input(XIN) Clock : 10MHz ● CPU Clock : 160MHz,max ● Bus Clock : 40MHz,max ● On-chip memory Flash Memory : 512KB RAM : 32KB
2	Memory	● SDRAM : 16-Mbyte EDS1216AATA-75E 1pc. (16-bit bus width) ● SRAM : 2-Mbyte (SRAM with byte selection) R1LV1616RSA7S 1pc. (16-bit bus width) ● EEPROM : 128k-bit HN58X24128FPIE 1pc. (I^2C Bus Connection)
3	Connector	● Extension Connector(Bus, I/O, VCC, GND) ● A/D, D/A Connector (AN0~7,DA0~1,AVcc,AVss,AVref,AVrefvss) ● Serial Port Connector (D-sub 9pins) ● H-UDI connector (14pins) ● H-UDI connector (36pins)
4	LED	● POWER LED (1pc.) ● User LED (6pcs.)
5	Switch	● Reset Switch (1pc.) ● NMI Switch (1pc.) ● IRQ3 Switch (1pc.) ● TP Switch (1pc.) ● DIP Switch for System Setting (1pc., 3 poles) ● DIP Switch for User (1pc., 4 poles)
6	Package Dimension	● Dimensions :100mm x 100mm ● Mounting Form :6-layer, Double-Side Mounted ● Board Configuration :1 board

1.4 External View

Figure1.4.1 shows the external view of M3A-HS11.

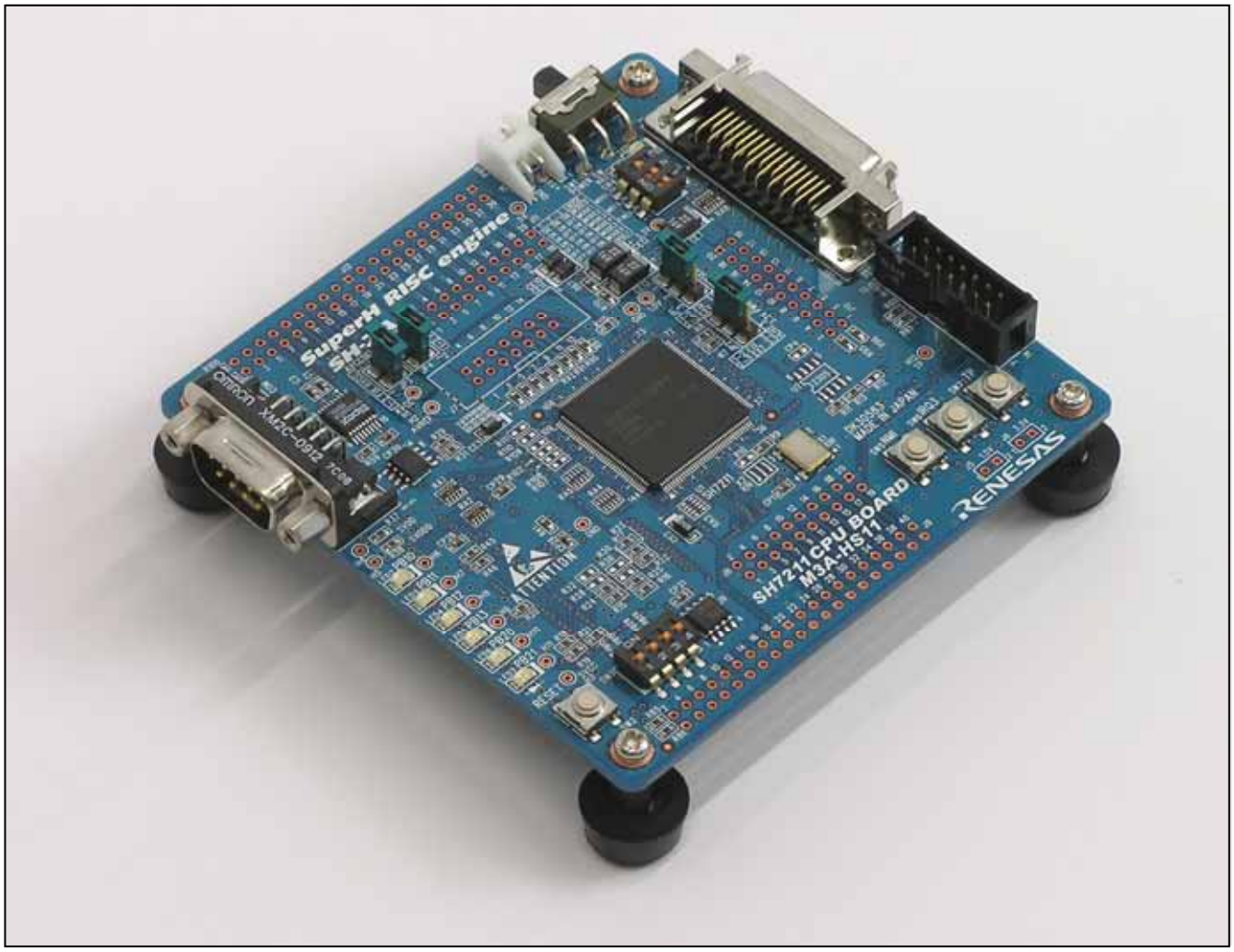


Figure1.4.1 External View of M3A-HS11

1.5 M3A-HS11 Block Diagram

Figure1.5.1 shows the system block diagram of M3A-HS11.

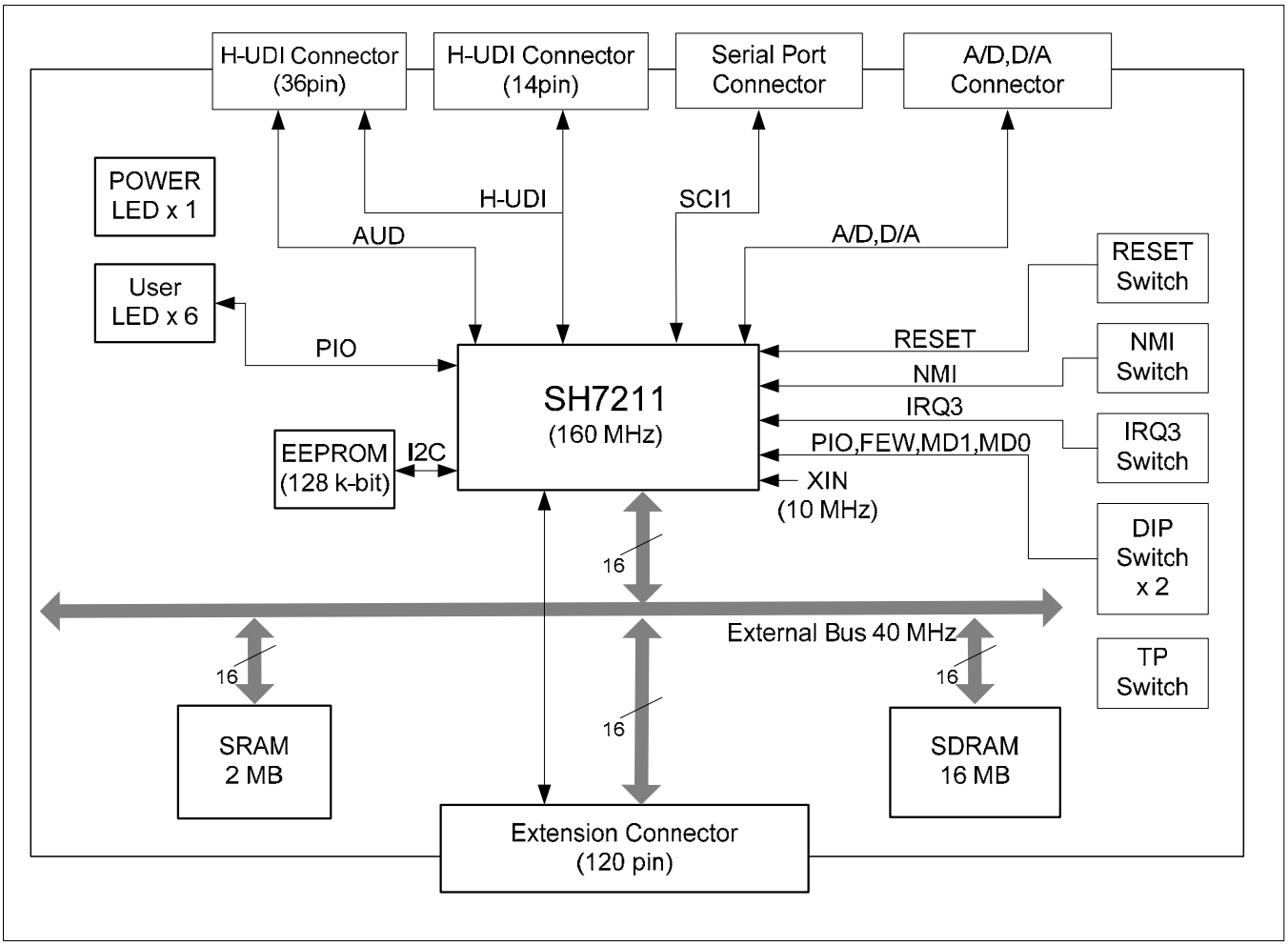
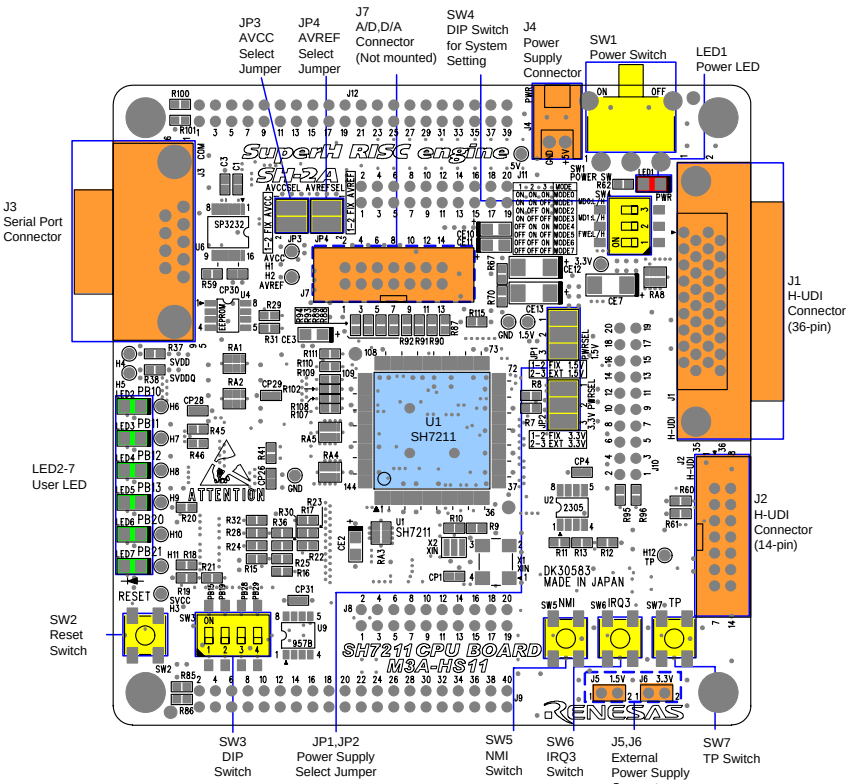


Figure1.5.1 System Block Diagram of M3A-HS11

1.6 M3A-HS11 Board Overview

Figure1.6.1 shows the M3A-HS11 board overview.

< Top view of the component side >



< Top view of the solder side >

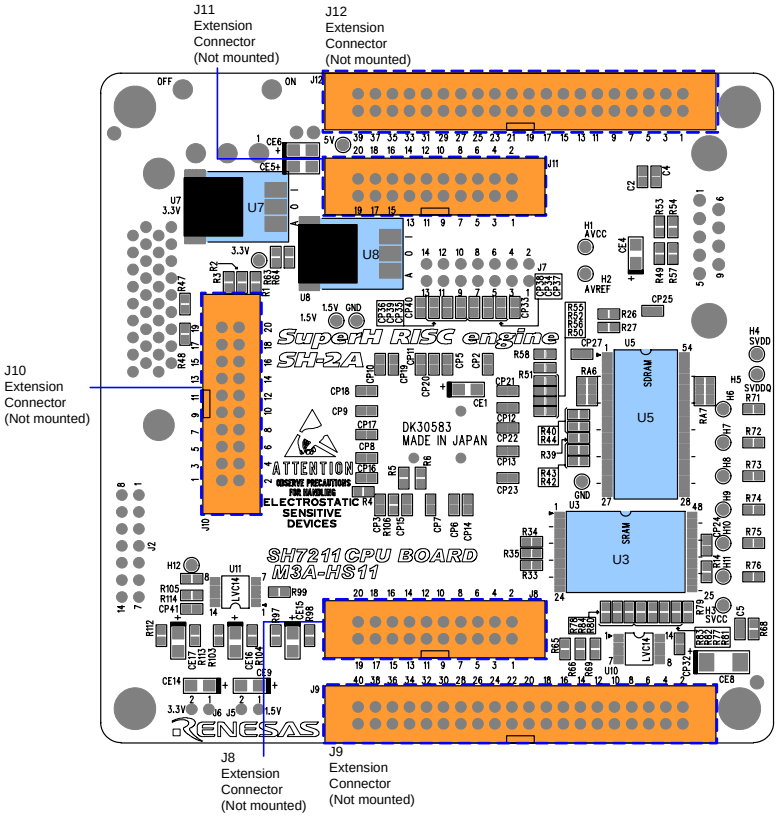


Figure1.6.1 M3A-HS11 Board Overview

Table1.6.1 lists main components mounted in the M3A-HS11.

Table1.6.1 Main Components Mounted in the M3A-HS11

Symbol	Parts Name	Remarks	Recommended Parts Number for Not-Mounted Components
U1	CPU	SH7211 (Renesas)	
U2	Clock Buffer	Not mounted	CY2305SC-1 (Cypress)
U3	SRAM	R1LV1616RSA7S	
U4	EEPROM	HN58X24128FPIE	
U5	SDRAM	EDS1216AATA-75E	
U6	RS-232C Driver	SP3232ECA(Sipex)	
U7	3.3V Voltage Regulator	LMS1587CSX-ADJ(NS)	
U8	1.5V Voltage Regulator	LMS1587CSX-ADJ(NS)	
U9	Reset IC	M51957BFP (Renesas)	
U10, U11	Logic IC		
X1	Oscillator	10.00MHz	
X2	Ceramic Resonator	Not mounted	CSTCE-G10M0 (Murata)
J1	H-UDI Connector	36-pin type	
J2	H-UDI Connector	14-pin type	
J3	Serial Port Connector		
J4	Power Supply Connector		
J5	External Power Supply Connector	Not mounted	A2-2PA-2.54DSA (Hirose)
J6	External Power Supply Connector	Not mounted	A2-3PA-2.54DSA (Hirose)
J7	A/D, D/A Connector	Not mounted	7614-6002 (Sumitomo 3M)
J8, J10, J11	Extension Connector	Not mounted	XG4C-2031 (Omron)
J9, J12	Extension Connector	Not mounted	XG4C-4031 (Omron)
LED1	Power LED	Red	
LED2-7	User LED	Green	
SW1	Power Switch		
SW2	Reset Switch		
SW3	DIP Switch for User		
SW4	DIP Switch for System Setting		
SW5	NMI Switch		
SW6	IRQ3 Switch		
SW7	TP Switch		

1.7 M3A-HS11 Memory Mapping

Figure1.7.1, Figure1.7.2 and Figure1.7.3 show the SH7211 memory mapping examples in the M3A-HS11 on each MCU mode.

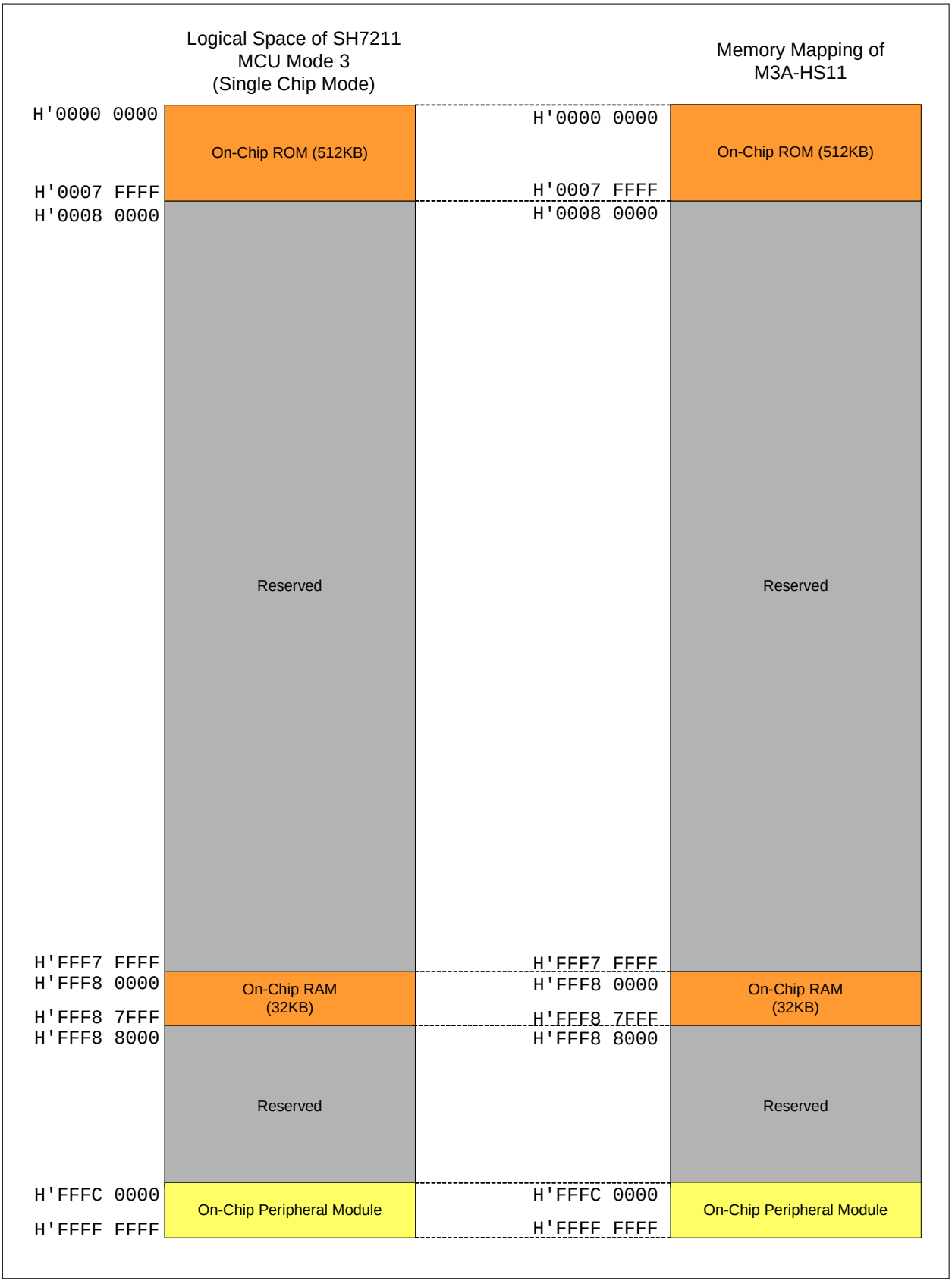


Figure1.7.1 SH7211Memory Mapping (MCU Mode 3)

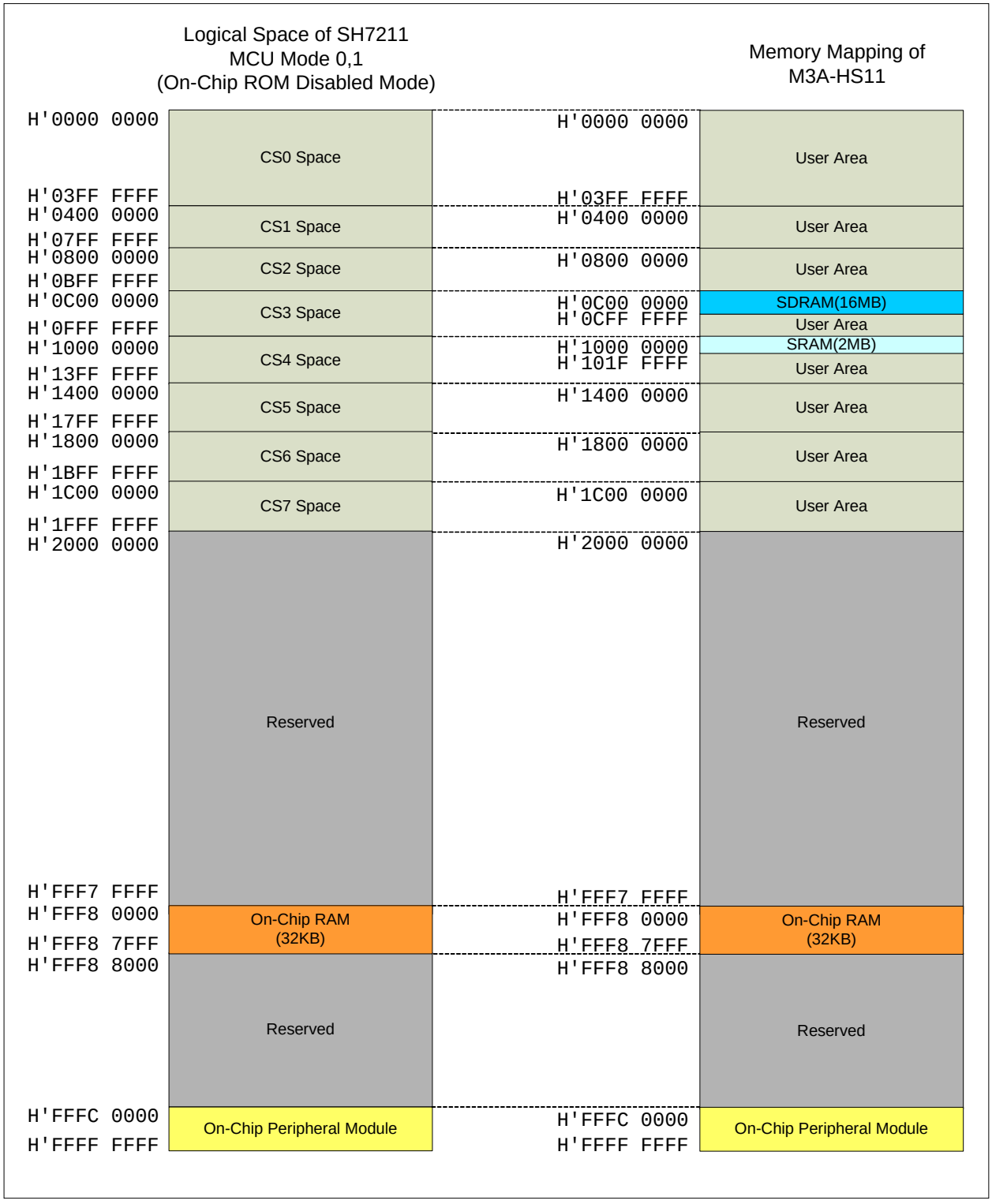


Figure1.7.2 SH7211Memory Mapping (MCU Mode 0,1)

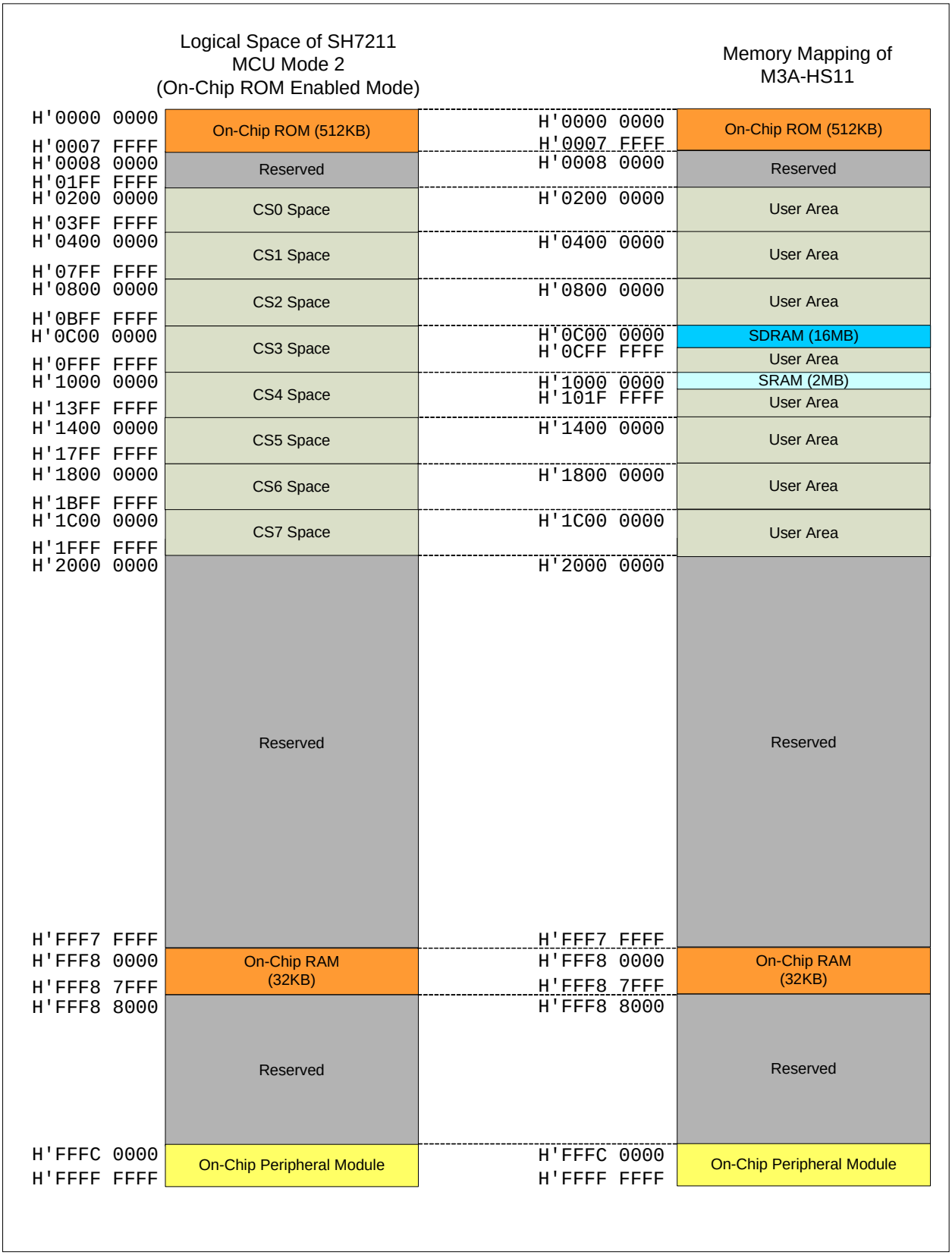


Figure1.7.3 SH7211Memory Mapping (MCU Mode 2)

1.8 Absolute Maximum Ratings

Table1.8.1 lists the absolute maximum ratings of M3A-HS11.

Table1.8.1 Absolute Maximum Ratings of M3A-HS11

Symbol	Parameter	Rated Value	Remarks
5VCC	5V System Power Supply Voltage	-0.3V to 6.0V	Relative to VSS
3VCC	3.3V System Power Supply Voltage	-0.3V to 4.6V	Relative to VSS
1.5VCC	1.5V System Power Supply Voltage	-0.3V to 2.3V	Relative to VSS
Topr	Operating Ambient Temperature	-10°C to 55°C	No dewdrops allowed. Use in corrosive gas environment prohibited.
Tstr	Storage Ambient Temperature	-20°C to 60°C	No dewdrops allowed. Use in corrosive gas environment prohibited.

Note: The ambient temperature refers to the air temperature in places closest possible to the board.

1.9 Recommended Operating Conditions

Table1.9.1 lists the recommended operating conditions of M3A-HS11.

Table1.9.1 Recommended Operating Conditions of M3A-HS11

Symbol	Parameter	Rated Value	Remarks
5VCC	5V System Power Supply Voltage	4.75V to 5.25V	Relative to VSS
3VCC	3.3V System Power Supply Voltage	3.0V to 3.6V	Relative to VSS
1.5VCC	1.5V System Power Supply Voltage	1.4V to 1.6V	Relative to VSS
-	Maximum Current Consumption in the Board	Within 2A	
Topr	Operating Ambient Temperature	0°C to 50°C	No dewdrops allowed. Use in corrosive gas environment prohibited.

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Chapter2
Functional Overview

2.1 Functional Overview

The M3A-HS11 is the SH7211 CPU board that has the functions listed in Table2.1.1.
Table2.1.1 lists the functional modules of M3A-HS11.

Table2.1.1 Functional Modules of M3A-HS11

Section	Function	Content
2.2	CPU	SH7211 ● Input(XIN) Clock: 10 MHz ● CPU Clock: Maximum 160 MHz, ● Bus Clock: Maximum 40 MHz ● On-Chip Memory - Flash Memory: 512 KB - RAM : 32 KB
2.3	Memory	● SDRAM: 16-Mbyte EDS1216AATA-75E 1pc. (16-bit bus width) ● SRAM : 2-Mbyte (SRAM with byte selection) R1LV1616RSA7S 1pc. (16-bit bus width) ● EEPROM : 128k-bit HN58X24128FPIE 1pc. (I^2C Bus Connection)
2.4	Serial Port Interface	Connects SCI1 of the SH7211 to the serial port connector
2.5	I/O Ports	Connects to the input/output ports of the SH7211
2.6	Power Supply	Controls the system power supply of the M3A-HS11
2.7	Clock Module	Controls the system clock
2.8	Reset Module	Controls the device reset mounted on the M3A-HS11
2.9	Interrupt Switches	Connect to the NMI pin, IRQ3 pin and test port
2.10	E10A-USB Interface	SH7211 H-UDI/AUD interface
-	Operational Specifications	Connectors, Switches and LEDs ● SH7211 Extension Connector ● Switches and LEDs ● H-UDI Connector Detailed in Chapter 3.

2.2 CPU

The M3A-HS11 contains the 32-bit RISC microcomputer SH7211 that operates with a maximum 160MHz of CPU clock frequency. The SH7211 includes 512-Kbyte flash memory, and 32-Kbyte RAM, making it useful in a wide range of applications from data processing to equipment control.

The M3A-HS11 can be operated with a maximum 160MHz of CPU clock frequency (external bus 40MHz, max) using a 10MHz input clock. Figure 2.2.1 shows the SH7211 block diagram in the M3A-HS11.

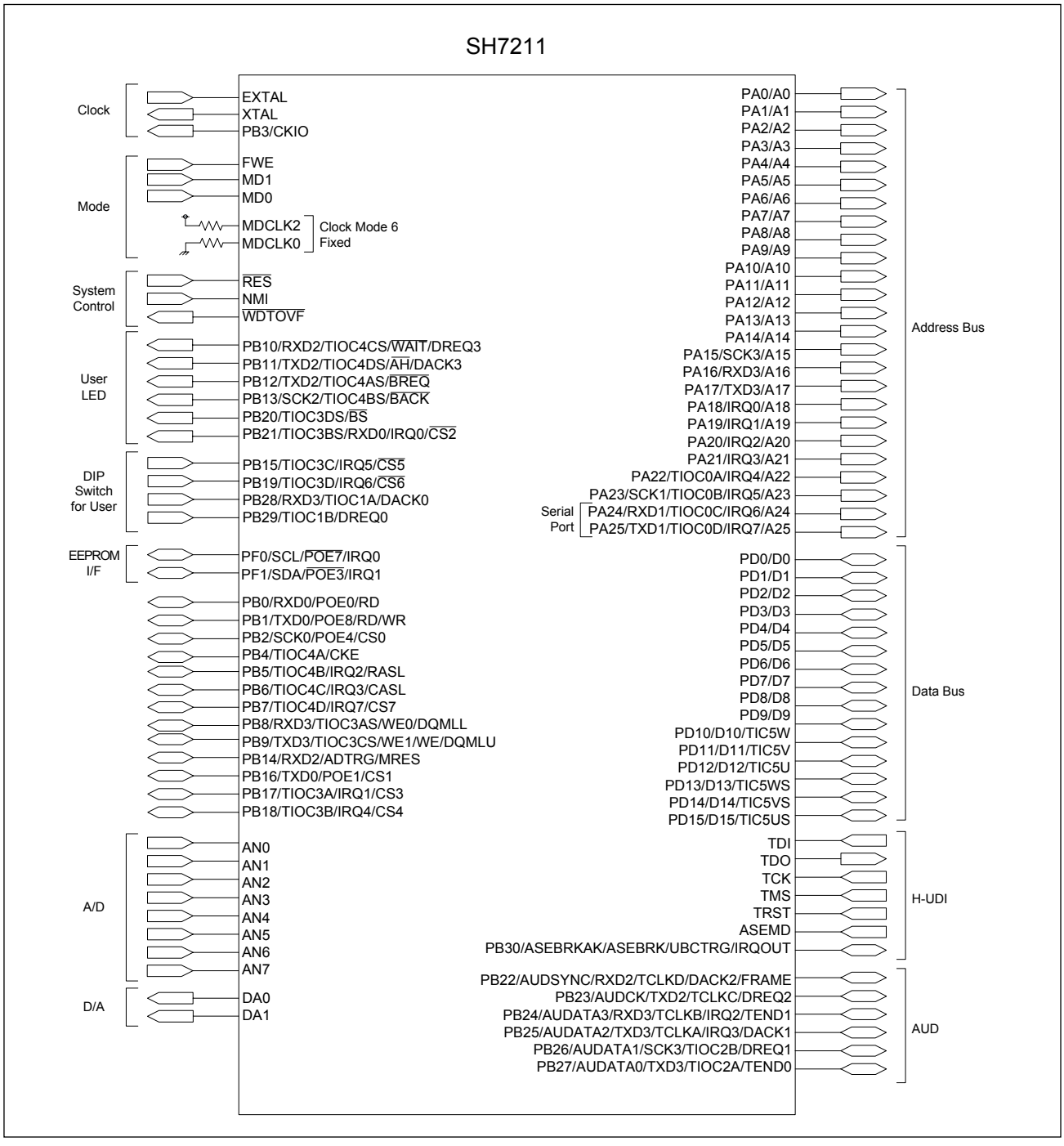

Figure 2.2.1 SH7211 Block Diagram

2.3 Memory

2.3.1 SH7211 On-Chip Memory

The SH7211 includes 512-Kbyte flash memory and 32-Kbyte RAM.

2.3.2 SDRAM

The M3A-HS11 mounts 16MB SDRAM as standard equipment. The SDRAM is controlled by the bus state controller built into SH7211. Table2.3.1 lists the SDRAM specifications used in M3A-HS11. Figure 2.3.1 shows the block diagram of SDRAM connection.

Table2.3.1 SDRAM Specifications

Specification	Content
Part Number	EDS1216AATA-75E
Configuration	16 Mbytes (16-bit bus width) x 1pc.
Capacity	16 Mbytes
Access Time	5.4ns
CAS Latency	2 (at 40 MHz bus clock)
Refresh Interval	4,096 refresh cycles every 64ms
Low Address	A11- A0
Column Address	A8 - A0
Number of Banks	4-bank operation controlled by BA0 and BA1

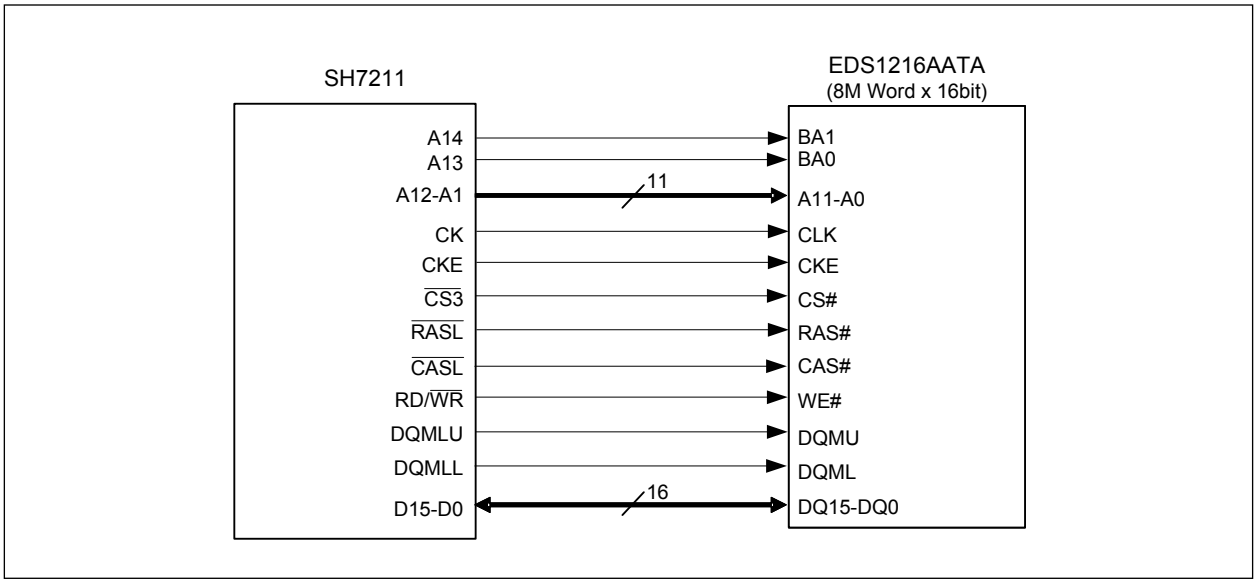

Figure 2.3.1 Block Diagram of SDRAM Connection

Table 2.3.2 lists the setting examples of bus state controller when the SH7211 bus clock is operating at 40 MHz.

Table 2.3.2 Setting Examples of Bus State Controller (CS3 Space)

User Area	Target Device	SDRAM Controller Setting
CS3	EDS1216AATA-75E	**CS3 Space Bus Control Register(CS3BCR)** Initial value: H'36DB 0600, Recommended set value: H'1000 4400 - Idle cycles between write-read cycles and write-write cycles IWW[2:0] = 001; 1 idle cycle inserted - Memory type TYPE[2:0] = 100; SDRAM - Data bus size BSZ[1:0] = 10; 16-bit size **CS3 Space Wait Control Register(CS3WCR)** Initial value: H'0000 0500, Recommended set value: H'0000 0000 0091 - Wait precharge completion cycle count WTRP[1:0] = 00; No wait cycle - Number of wait cycles from ACTV to READ/WRIT command WTRCD[1:0] = 00; No wait cycle - Area 3 CAS latency A3CL[1:0] = 01; 2 cycles - Number of command cycle from WRIT(A) to auto-precharge/PRE command TRWL[1:0] = 10; 2 cycles Number of command cycle from REF command/self-refresh release to ACTV command WTRC[1:0] =01; 3 cycles **SDRAM Control Register(SDCR)** Initial value: H'0000 0000, Recommended set value: H'0000 0809 - Refresh control RFSH = 1; Refresh is performed - Refresh control RMODE = 0; Auto-refreshing - Bank active mode BACTV = 0; Auto-precharge mode - Number of bits of row address for area3 A3ROW[1:0] = 01; 12 bits - Number of bits of column address for area3 A3COL[1:0] = 01; 9 bits **Refresh Timer Control/Status Register(RTCSR)** Initial value : H'0000 0000, Recommended set value : H'A55A 0010 - Clock select CKS[2:0] = 010 ;Bϕ/16 - Refresh count RRC[2:0] = 000 ; Once **Refresh Time Constant Register(RTCOR)** Initial value: H'0000 0000, Recommended set value : H'A55A 0027 *The refresh request interval when clock select is set to Bϕ/16 is as follows. 1 cycle :400nsec(40 MHz/16 = 2.5 MHz) Refresh request intervals in the SDRAM : 15.625μsec/time 15.625μsec /400nsec = 39(0x27) cycle / refresh counts

Figure 2.3.2 shows an example of SDRAM single read/write timing for operation that the SH7211 bus clock is operating at 40 MHz.

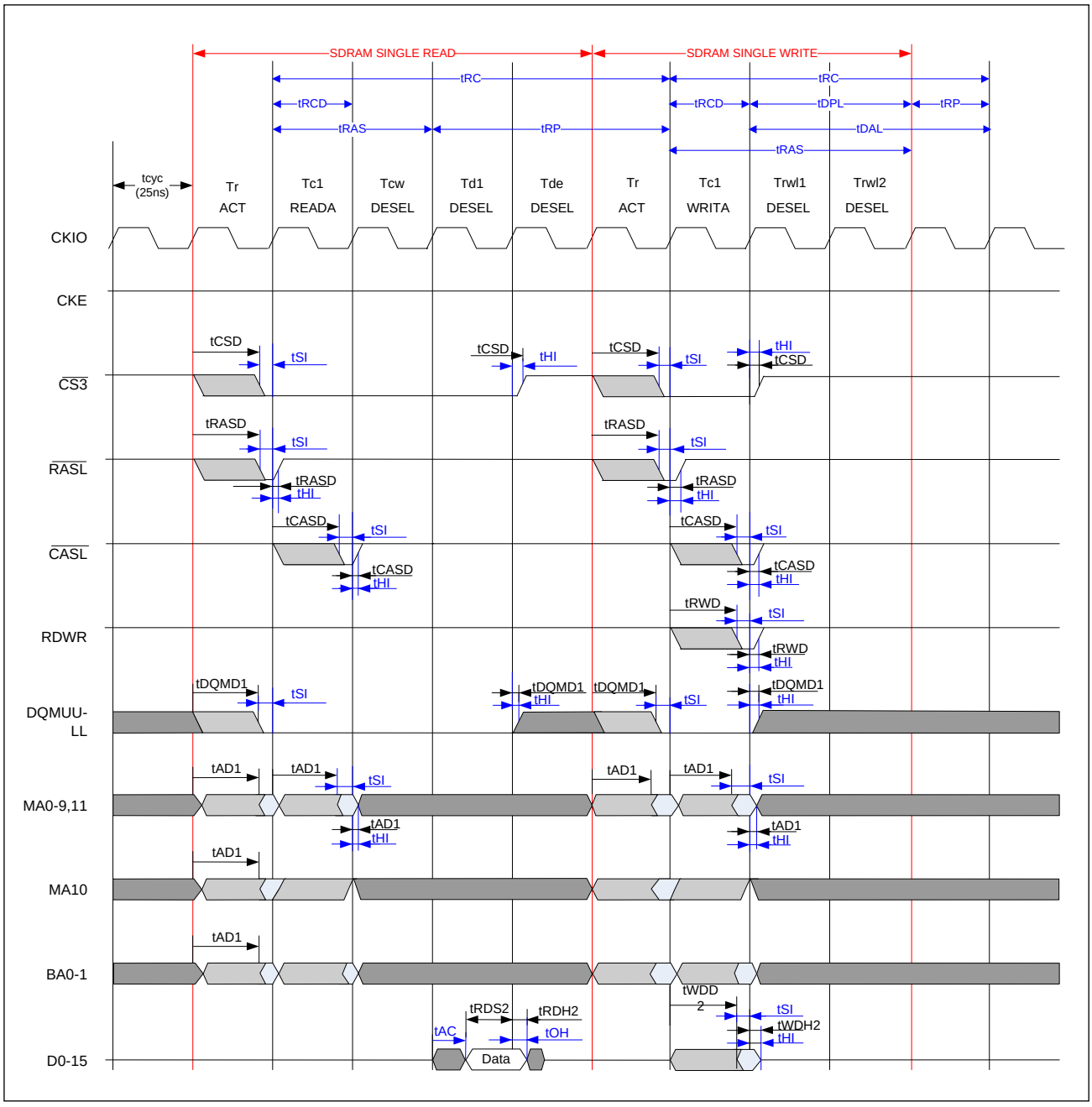

Figure 2.3.2 Example of SDRAM Single Read/Write Timing

2.3.3 SRAM

The M3A-HS11 includes the 2-Mbyte SRAM as standard equipment. The SRAM is controlled by the bus state controller included in SH7211.

Table2.3.3 lists the specification outline of SRAM. Figure 2.3.3 shows the block diagram of SH7211 and SRAM.

Table2.3.3 SRAM Specification Outline

Part Number	Bus Size	Capacity	Package
R1LV1616RSA-7S	16-bit	2-Mbyte (16-bit × 1M word × 1 pc.)	48-pin TSOP (20 ×12mm)

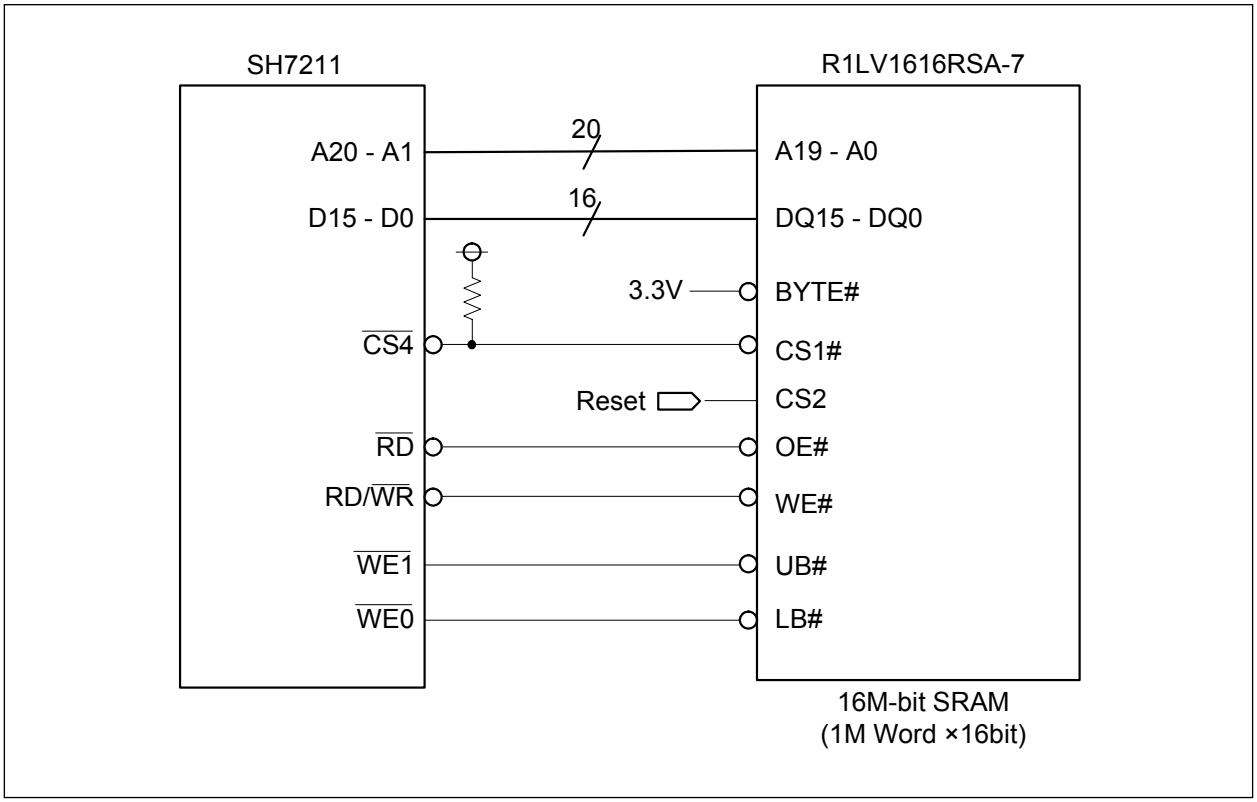

Figure 2.3.3 Block Diagram of SH7211 and SRAM

Table2.3.4 lists the setting example of bus state controller when the bus clock of SH7211 is operating at 40 MHz.

Table2.3.4 Setting Examples of Bus State Controller (CS4 Space)

User Area	Target Device	SDRAM Controller Settings
CS4	R1LV1616RSA-7S	**CS4 Space Bus Control Register : CS4BCR** Initial value : H'36DB 0400, Recommended value : H'1659 3400 • Idle cycles between write-read cycles and write-write cycles IWW[2:0] = 001 ; 1 idle cycle inserted • Idle cycles for another space read-write IWRWD[2:0] = 011 ; 4 idle cycle inserted • Idle cycles for read-write in same space IWRWS[2:0] = 001 ; 1 idle cycle inserted • Idle cycles for another space read-read IWRRD[2:0] = 011 ; 4 idle cycle inserted • Idle cycles for read-read in same space IWRRS[2:0] = 001 ; 1 idle cycle inserted • Specify memory type TYPE[2:0] = 011 ; Byte selection SRAM • Specify data bus type BSZ[1:0] = 10 ; 16 bit bus width **CS4 Space Wait Control Register : CS4WCR** Initial value: H'0000 0500, Recommended value: H' • Byte access selection for byte-selection SRAM BAS = 1 ; Asserts the WEn during the read/write access cycle and asserts the RDWR at the write timing. • Number of write access wait cycles WW[2:0] = 000 ; Same number of cycles as the number of read access wait • Number of delay cycles from address, CS4 assertion to RD, WEn assertion SW[1:0] = 01 ; 1.5 cycles • Number of read access wait cycles WR[3:0] = 0011 ; 3 cycles • External wait mask specification WM =1 ; External wait is ignored • Number of delay cycles from RD, WEn negation to address, CS4 negation HW[1:0] = 01 ; 1.5 cycles

Figure 2.3.4 shows the example of SRAM read timing when the bus clock is 40MHz and Figure 2.3.5 shows the example of SRAM write timing when the bus clock is 40MHz.

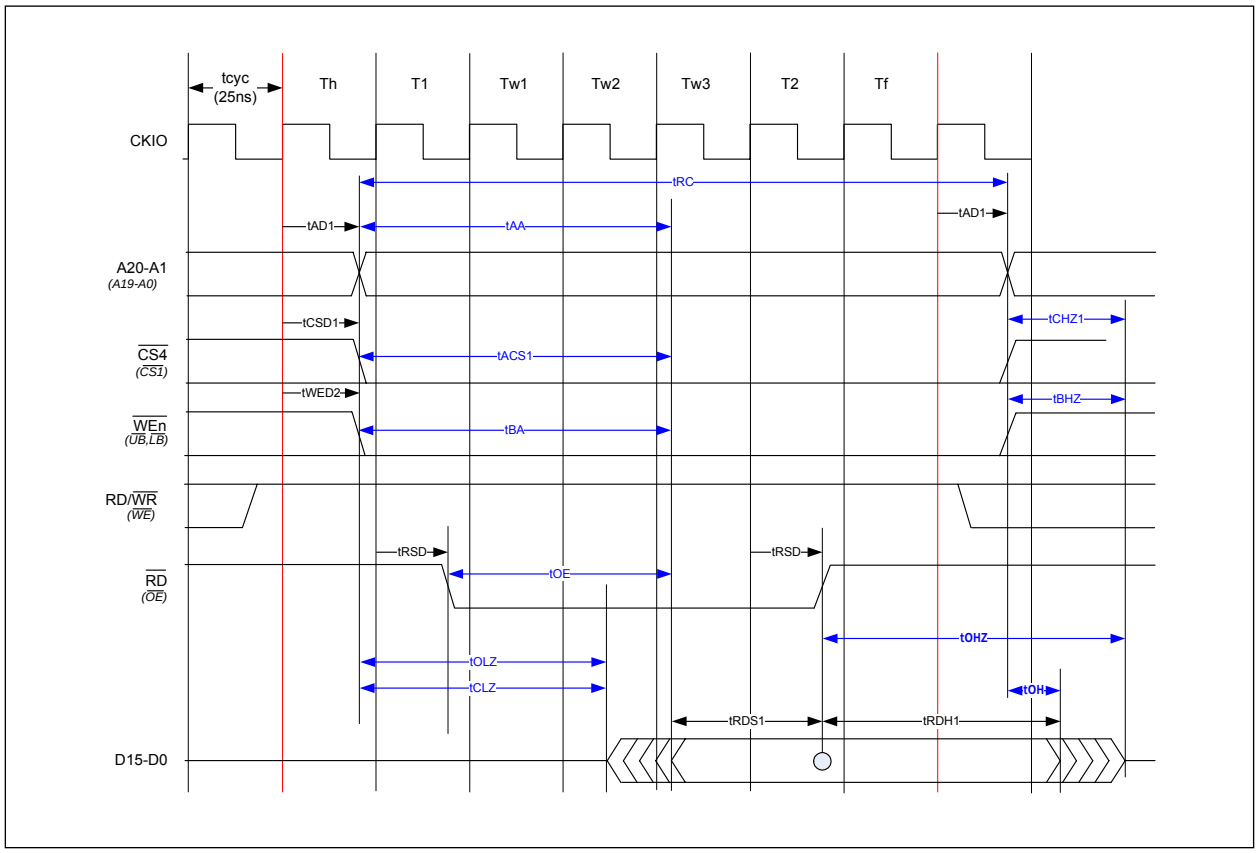

Figure 2.3.4 Example of SRAM Read Timing

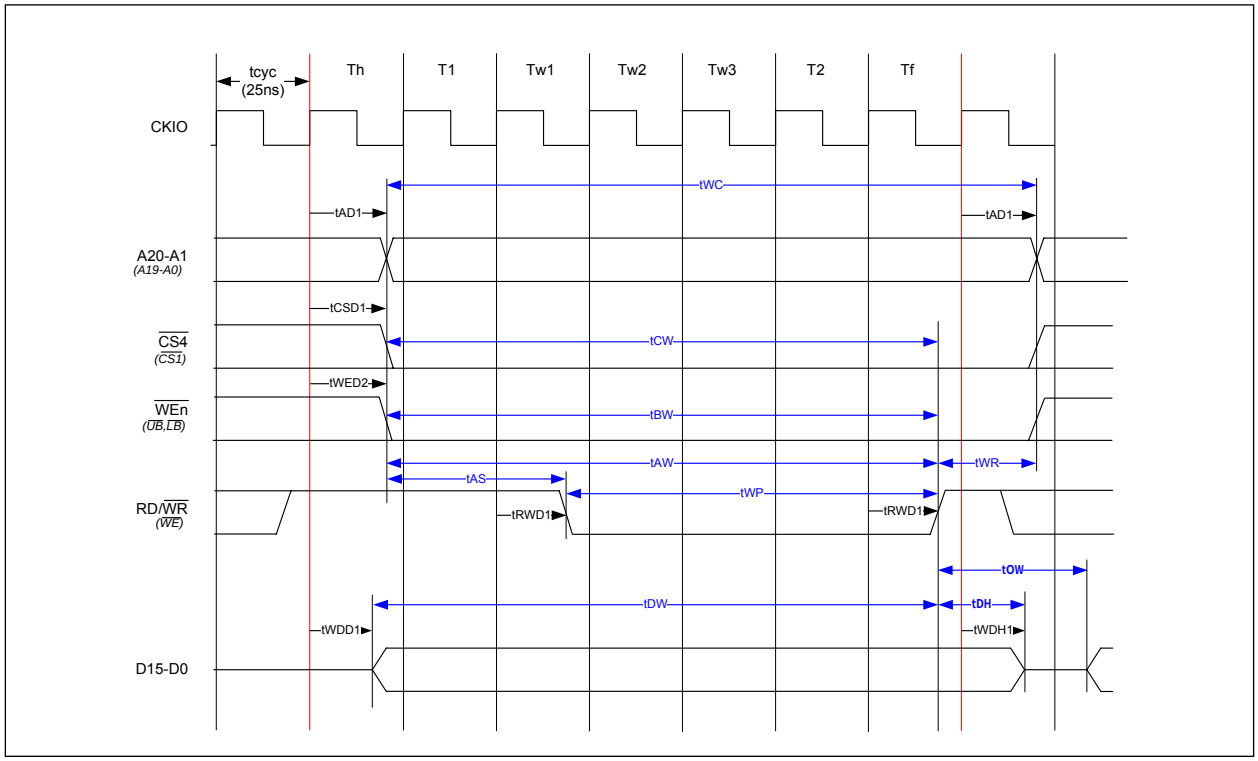

Figure 2.3.5 Example of SRAM Write Timing

2.3.4 EEPROM

The M3A-HS11 includes the 128k-bit EEPROM as standard equipment. The EEPROM is controlled by the I2C bus interface included in SH7211.

Table 2.3.5 lists the specification outline of EEPROM.

Figure 2.3.6 shows the connection circuit block diagram of SH7211 and EEPROM.

Table 2.3.5 EEPROM Specification Outline

Part Number	Interface	Capacity	Package
HN58X24128FPIE	2-wire system serial (I^2C bus)*1	128 k-bit (16k-word × 8-bit)	8-pin SOP

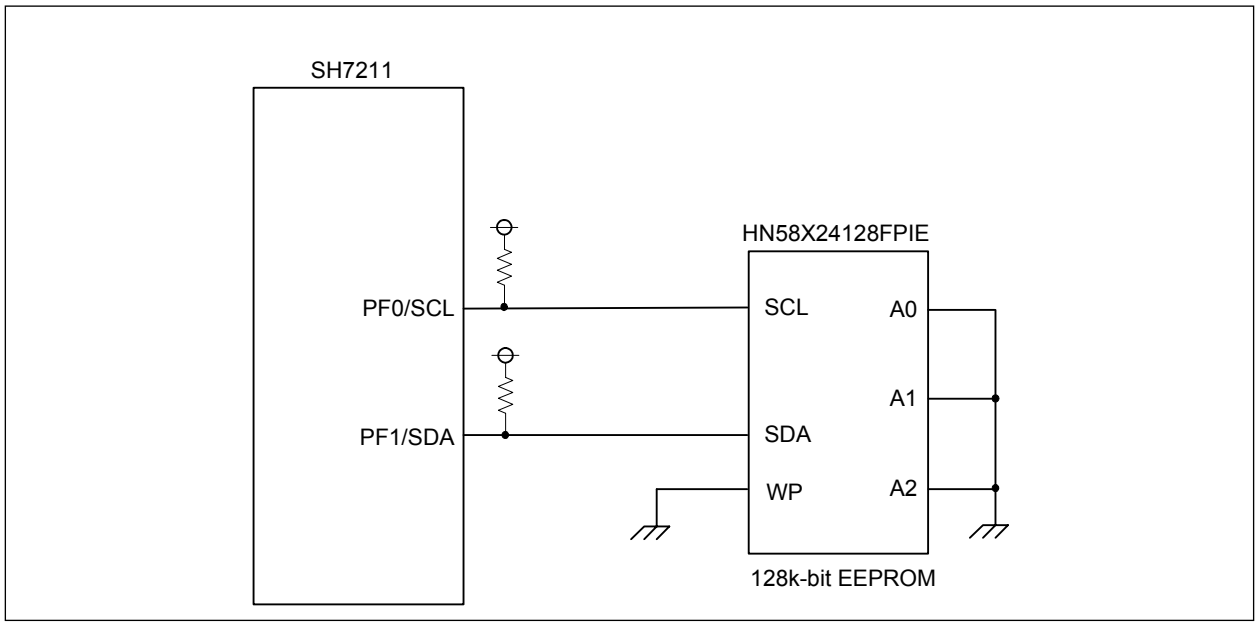

Figure 2.3.6 Block Diagram of SH7211 and EEPROM

Note*1: I^2C bus is a trademark of Koninklijke Philips Electronics N. V.

2.4 Serial Port Interface

In the M3A-HS11, the SCI channel 1 of SH7211 is connected to the serial port connector (J3).
Figure 2.4.1 shows the block diagram of serial port interface in the M3A-HS11.

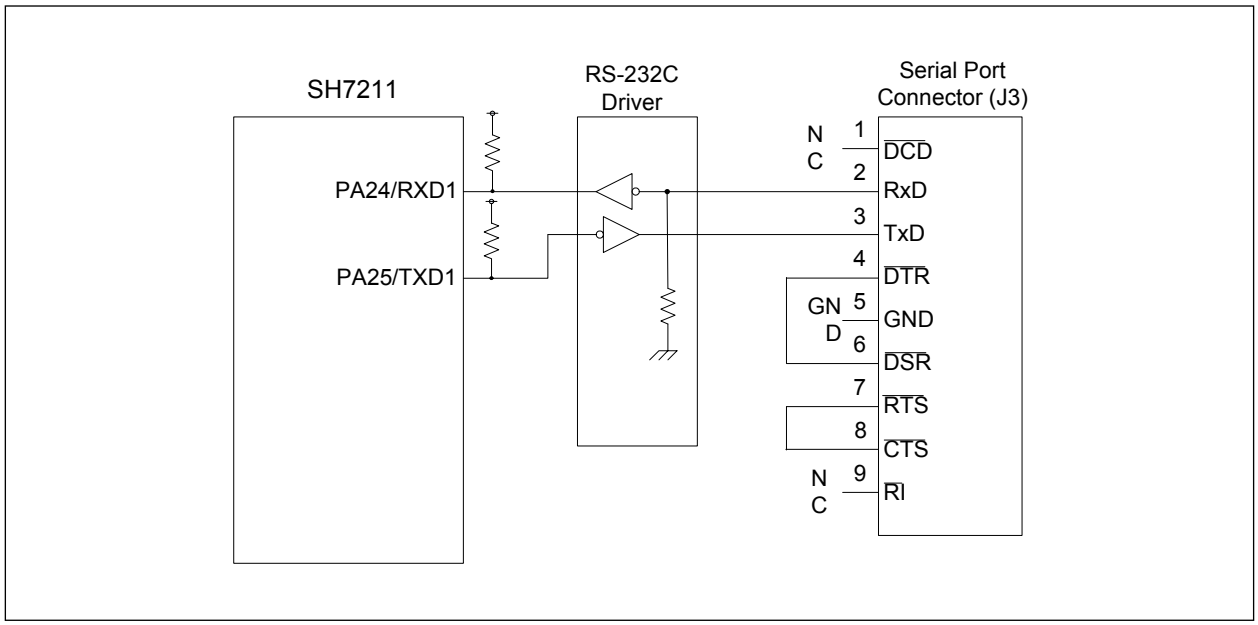

Figure 2.4.1 Block Diagram of Serial Port Interface

2.5 I/O Ports

In the M3A-HS11, all of the SH7211's I/O ports are connected to the extension bus connector.

Some I/O ports are connected to DIP switches and LEDs of the M3A-HS11 board. Users are free to use these ports.

Figure 2.5.1 shows the block diagram of DIP Switch and LEDs in the M3A-HS11.

Table 2.5.1 lists the functions of the SH7211 I/O ports in the M3A-HS11.

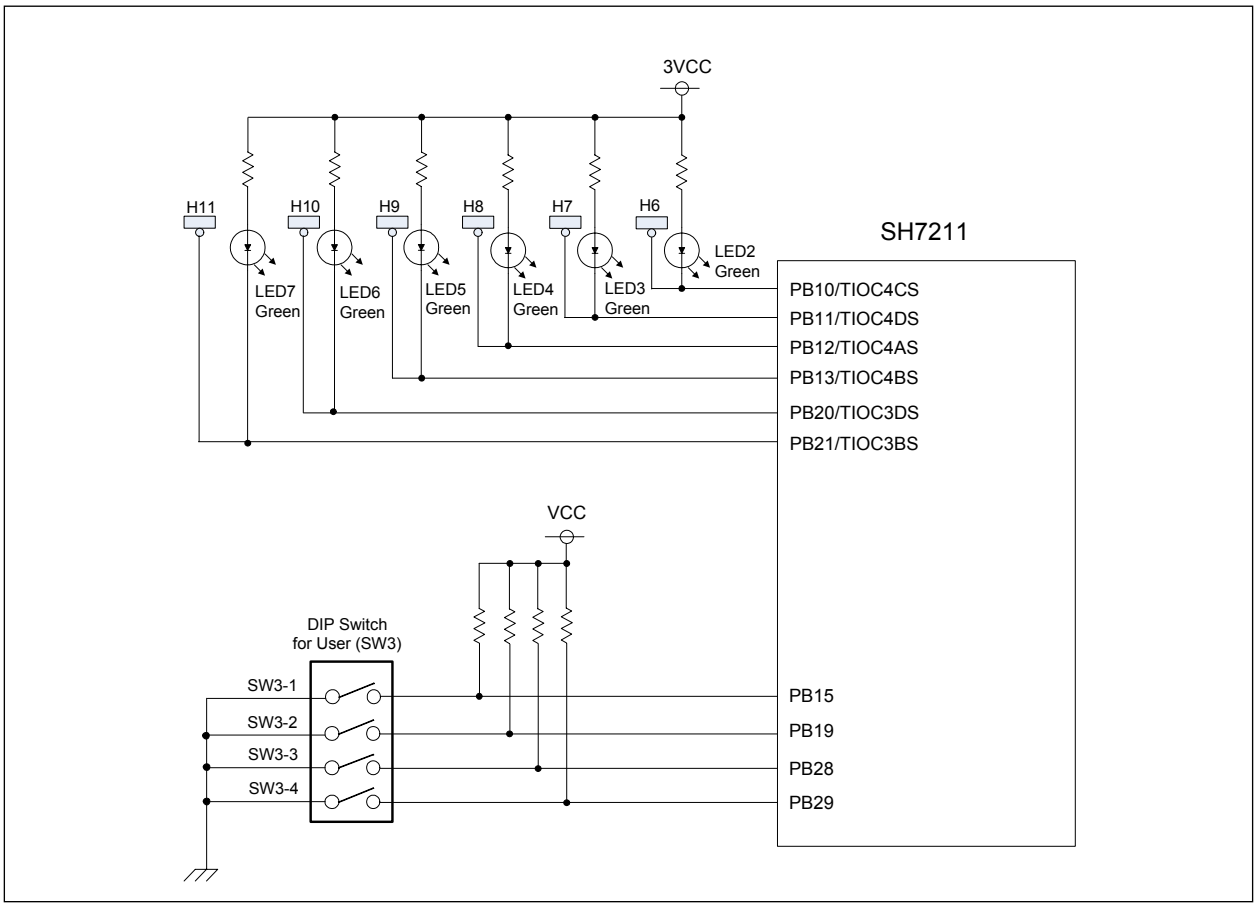

Figure 2.5.1 Block Diagram of DIP Switch and LEDs in M3A-HS11

Table 2.5.1 Functions of SH7211 I/O Ports

SH7211 Port Name	Connection in M3A-HS11
PA0	Extension Connector (J8, J9)
PA1 - PA9	Extension Connector (J8, J9), SDRAM, SRAM
PA10 - PA14	Extension Connector (J9), SDRAM, SRAM
PA15 - PA20	Extension Connector (J9), SRAM
PA21	Extension Connector (J9), IRQ3 Switch
PA22	Extension Connector (J9, J10)
PA23	Extension Connector (J9, J12)
PA24 - PA25	Extension Connector (J9), Serial Port Connector
PB0	Extension Connector (J11, J12) , SRAM
PB1	Extension Connector (J10), SDRAM, SRAM
PB2	Extension Connector (J8, J9, J12)
PB3	Extension Connector (J8, J9), SDRAM
PB4 - PB6	Extension Connector (J10), SDRAM
PB7	Extension Connector (J10, J12)
PB8 - PB9	Extension Connector (J10), SDRAM, SRAM
PB10	Extension Connector (J10, J12), LED
PB11	Extension Connector (J10), LED
PB12 - PB13	Extension Connector (J10, J12), LED
PB14	Extension Connector (J12)
PB15	Extension Connector (J8, J9, J12), DIP Switch for User
PB16	Extension Connector (J8, J9)
PB17	Extension Connector (J10), SDRAM
PB18	Extension Connector (J8, J9), SRAM
PB19	Extension Connector (J10), DIP Switch for User
PB20	Extension Connector (J12), LED
PB21	Extension Connector (J8, J9), LED
PB22 - PB27, PB30	(It is possible to connect to the extension connector (J12) by mounting the resistance)
PB28 - PB29	Extension Connector (J12), DIP Switch for User
PD0 - PD15	Extension Connector (J11, J12)
PF0 - PF1	Extension Connector (J10), EEPROM

2.6 Power Supply Circuit

In the M3A-HS11, the 5V power supply is input to the board and it generates 3.3V and 1.5V by using a regulator.

The used regulator uses an output voltage-controlled type so that a desired voltage value can be generated by changing the resistance.

Figure 2.6.1 shows the block diagram of power supply circuit in the M3A-HS11.

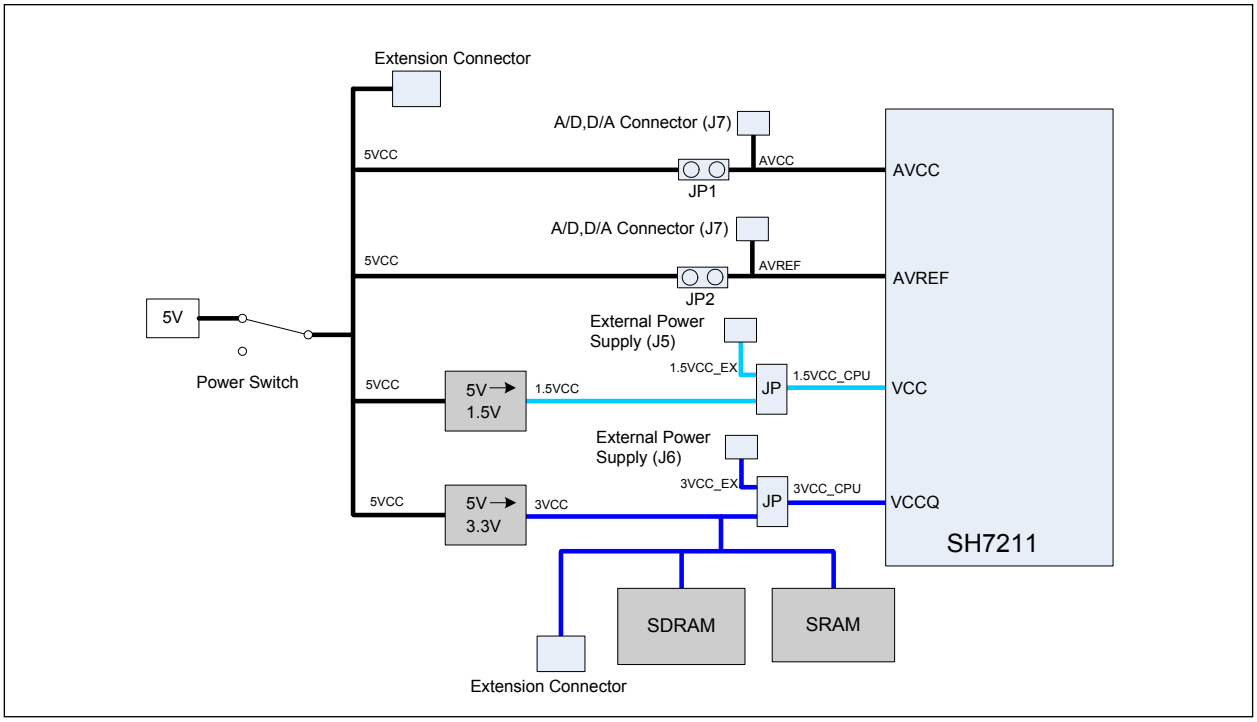

Figure 2.6.1 Block Diagram of Power Supply Circuit

2.7 Clock Module

The clock module in the M3A-HS11 consists of the following two blocks:

- Output from a oscillator connected to EXTAL of the SH7211
- Ceramic resonator connected to EXTAL and XTAL

The M3A-HS11 has a 10MHz oscillator connected to it as standard specification.

System clock output (PB3/CKIO) of SH7211 is connected to an extension connector with dumping resistor.

To connect an extension board to the extension connector, it is recommended to install a clock buffer that contains a PLL to ensure that the board will be supplied with a stable clock signal.

Figure 2.7.1 shows the block diagram of clock module.

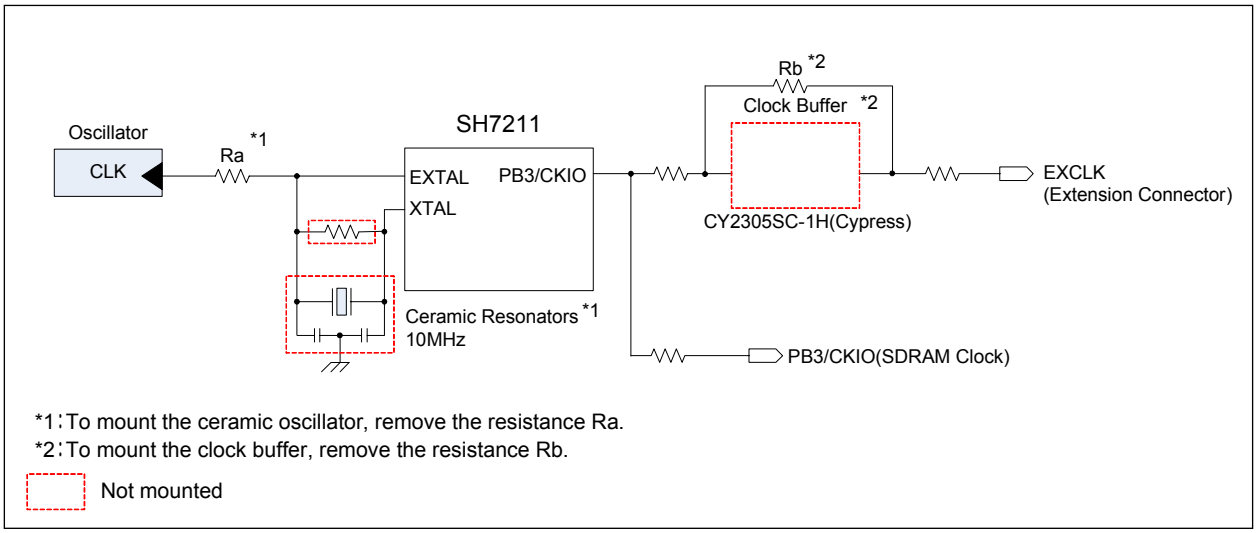

Figure 2.7.1 Block Diagram of Clock Module

2.8 Reset Module

This circuit controls the reset signal of SH7211 mounted on the M3A-HS11.

Figure 2.8.1 shows the block diagram of reset module in the M3A-HS11.

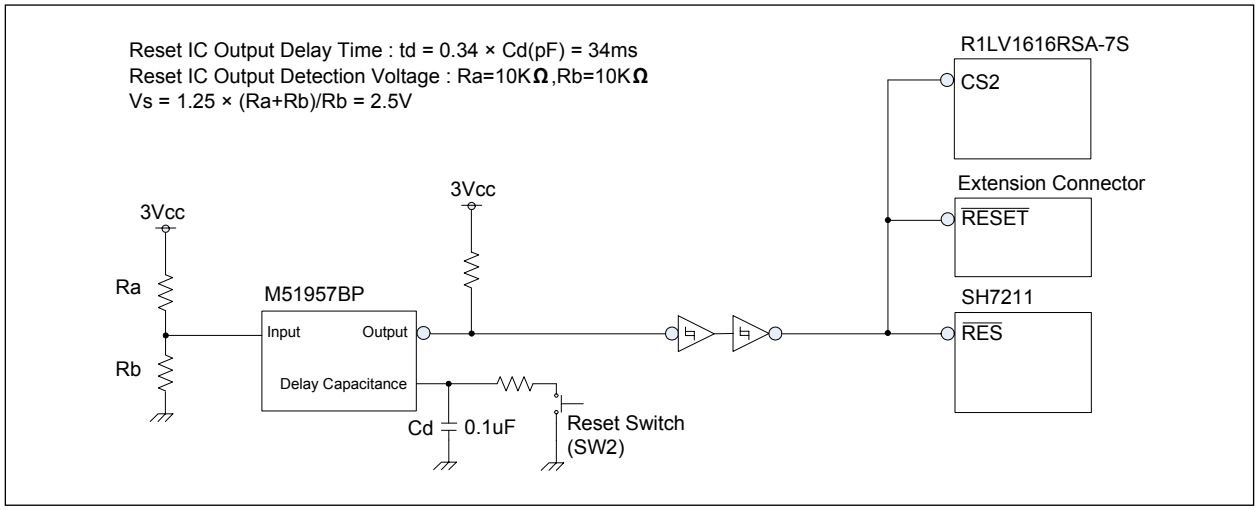

Figure 2.8.1 Block Diagram of Reset Module

2.9 Interrupt Switches

In the M3A-HS11, the push switches are connected with the IRQ3 (PA21) pin and NMI pin of the SH7211. Moreover, TP switch is connected with the test port (H12) so that it can be used by connecting with a desired pin. Figure 2.9.1 shows the block diagram of interrupt switch in the M3A-HS11.

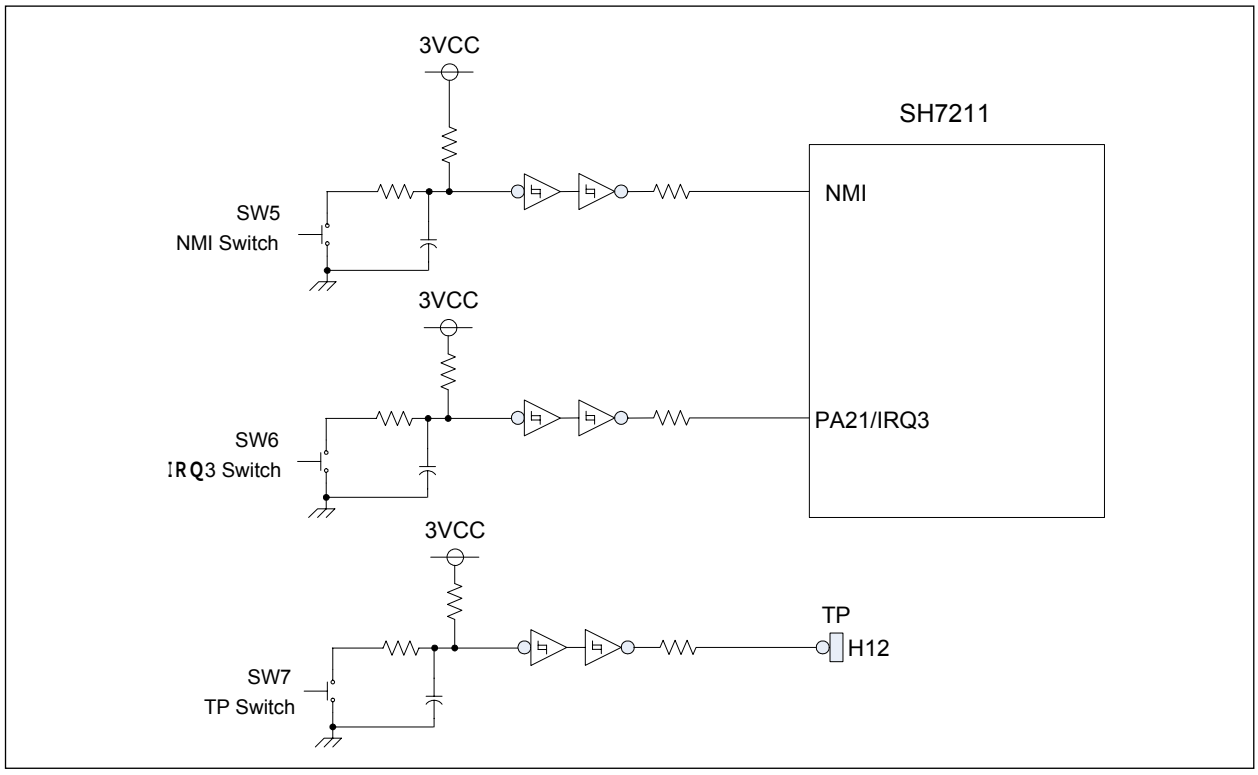

Figure 2.9.1 Block Diagram of Interrupt Switch

2.10 E10A-USB Interface

The M3A-HS11 has the H-UDI connectors (14-pin and 36-pin) to connect with E10A-USB.

Figure 2.10.1 shows the block diagram of E10A-USB interface.

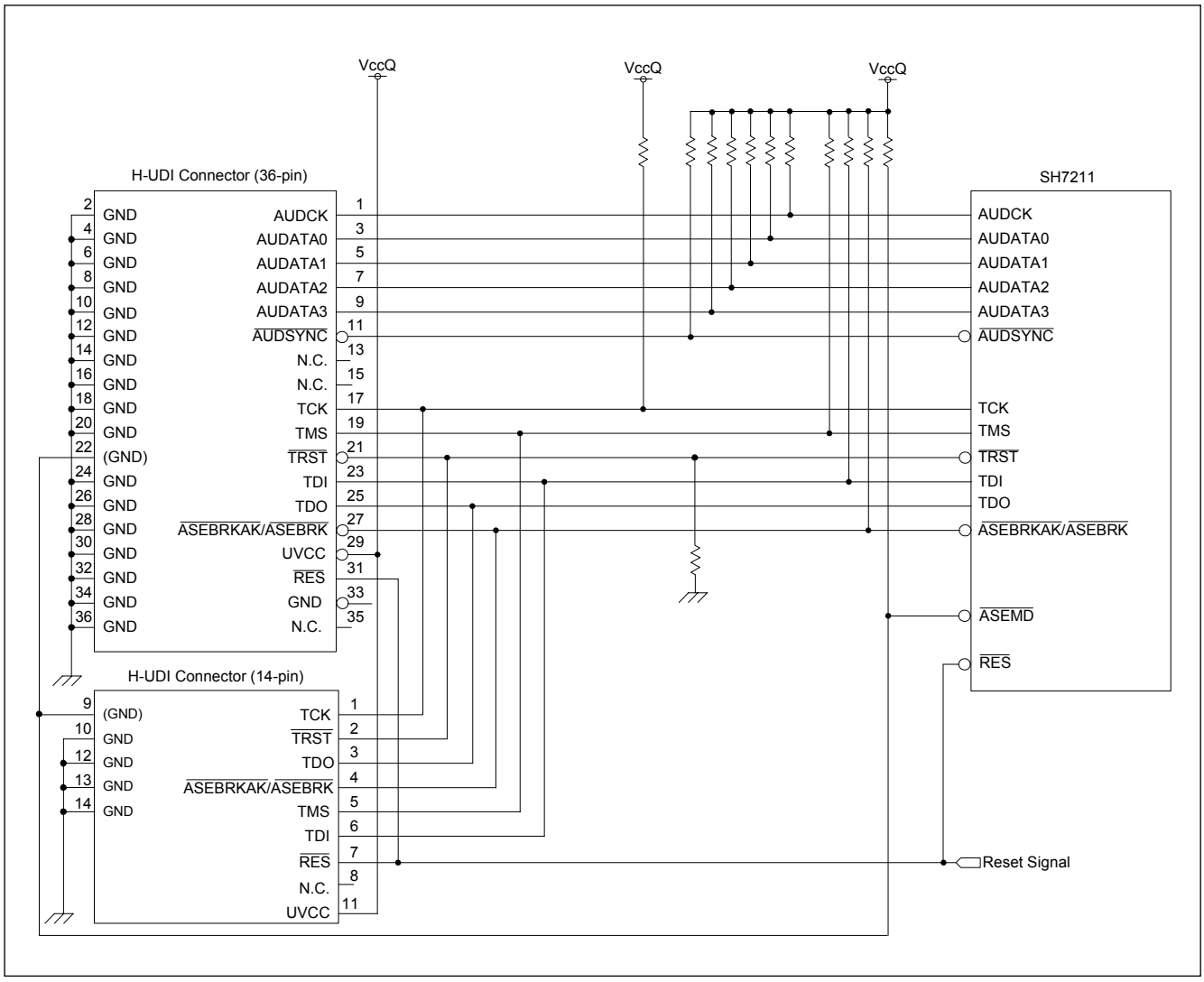

Figure 2.10.1 Block Diagram of E10A-USB Interface

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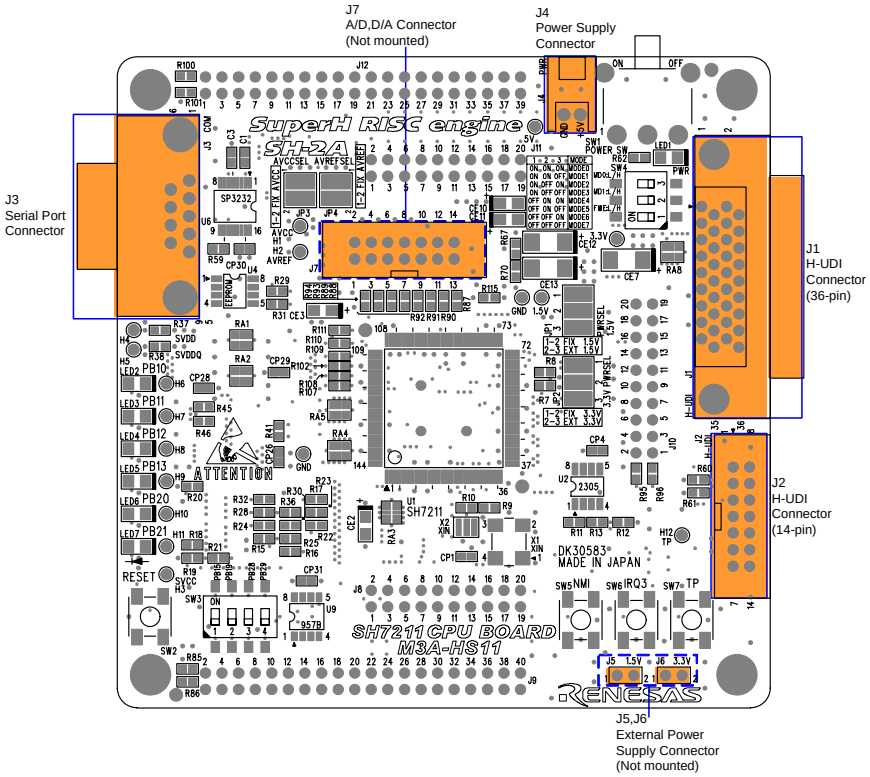
Chapter 3
Operational Specifications

3.1 M3A-HS11 Connectors Outline

Figure 3.1.1 shows M3A-HS11 connector assignments.

<Top View of the Component Side >



< Top View of the Solder Side >

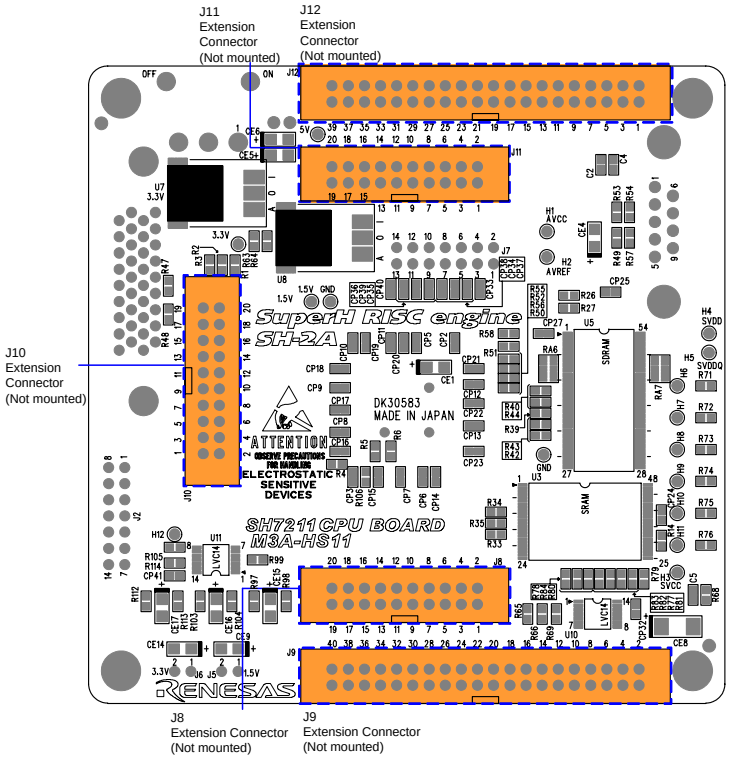


Figure 3.1.1 M3A-HS11 Connector Assignments

3.1.1 H-UDI Connector (J1, J2)

The M3A-HS11 includes a 36-pin H-UDI (J1) connector and 14-pin H-UDI (J2) connector for a connection to the E10A-USB emulator.

Figure 3.1.2 shows a pin assignment of H-UDI (J1) connector.

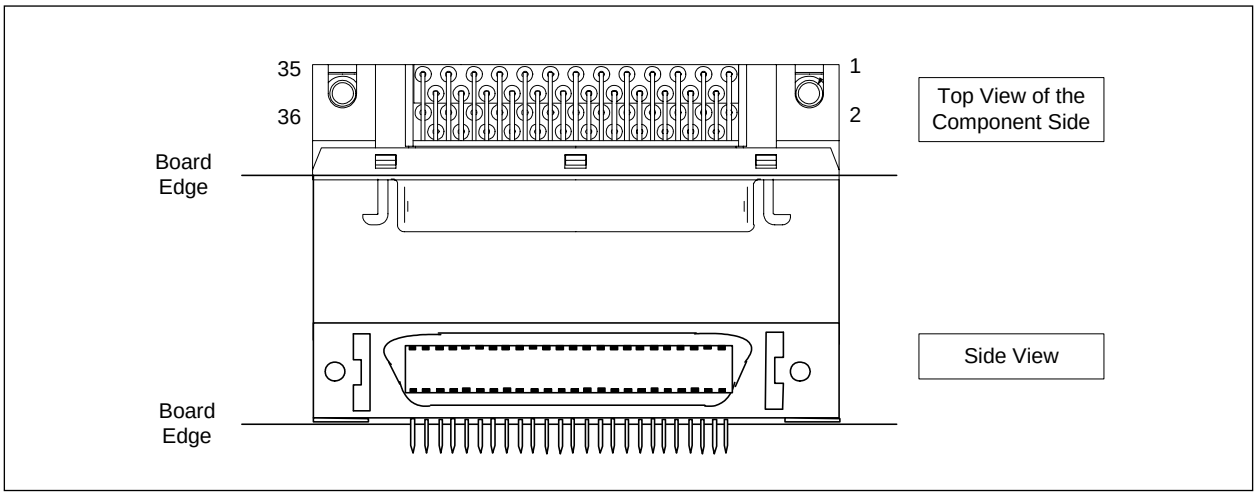


Figure 3.1.2 Pin Assignment of H-UDI(J1) Connector

Table 3.1.1 lists pin assignments of H-UDI connector (J1).

Table 3.1.1 Pin Assignments of H-UDI (J1) Connector

Pin	Signal Name	Pin	Signal Name
1	AUDCK	19	TMS
2	GND	20	GND
3	AUDATA0	21	$\overline{\text{TRST}}$
4	GND	22	(GND)
5	AUDATA1	23	TDI
6	GND	24	GND
7	AUDATA2	25	TDO
8	GND	26	GND
9	AUDATA3	27	$\overline{\text{ASEBRKAK/ASEBRK}}$
10	GND	28	GND
11	$\overline{\text{AUDSYNC}}$	29	UVCC
12	GND	30	GND
13	NC	31	$\overline{\text{RES}}$
14	GND	32	GND
15	NC	33	GND
16	GND	34	GND
17	TCK	35	NC
18	GND	36	GND

Figure 3.1.3 shows a pin assignment of H-UDI (J2) connector.

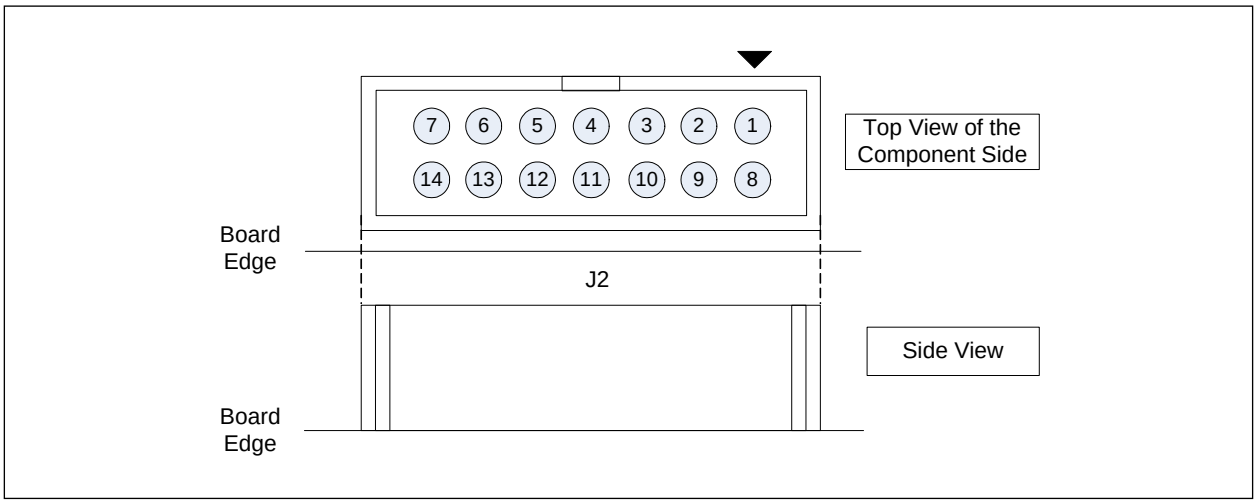


Figure 3.1.3 Pin Assignment of H-UDI (J2) Connector

Table 3.1.2 lists pin assignments of H-UDI (J2) connector.

Table 3.1.2 Pin Assignments of H-UDI (J2) Connector

Pin	Signal Name	Pin	Signal Name
1	TCK	8	NC
2	$\overline{\text{TRST}}$	9	(GND)
3	TDO	10	GND
4	$\overline{\text{ASEBRKAK/ASEBRK}}$	11	UVCC
5	TMS	12	GND
6	TDI	13	GND
7	$\overline{\text{RES}}$	14	GND

3.1.2 Serial Port Connector (J3)

The M3A-HS11 includes a serial port connector (J3).

Figure3.1.4 shows a pin assignment of serial port connector.

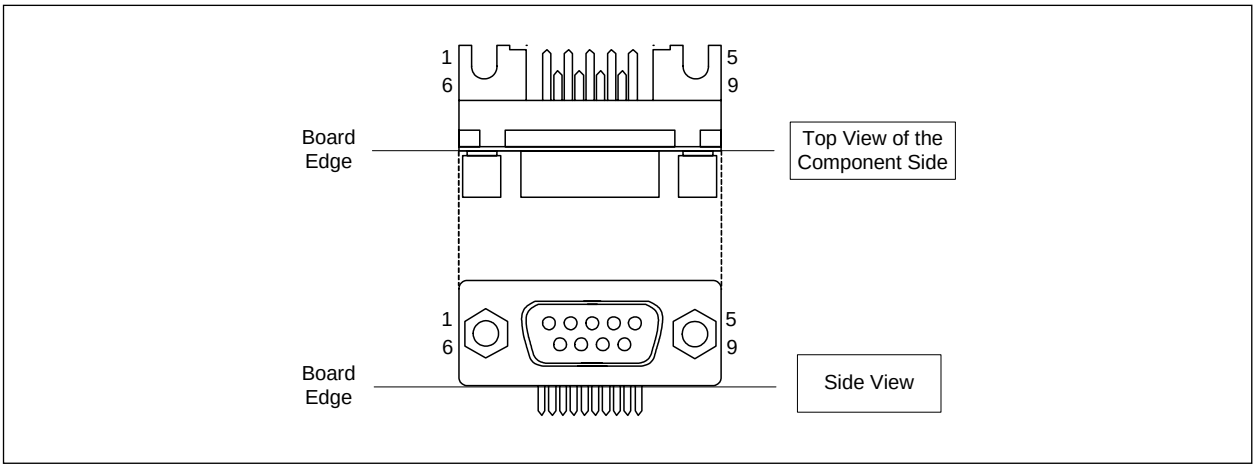


Figure3.1.4 Pin Assignment of Serial Port Connector (J3)

Table 3.1.3 lists pin assignments of serial port connector.

Table 3.1.3 Pin Assignments of Serial Port Connector (J3)

Pin	Signal Name	Pin	Signal Name
1	NC	6	$\overline{\text{DSR}}$
2	RXD	7	$\overline{\text{RTS}}$
3	TXD	8	$\overline{\text{CTS}}$
4	$\overline{\text{DTR}}$	9	NC
5	GND		

Pins 4-6 are loop back connected. Pins 7-8 are loop back connected.

3.1.3 Power Supply Connector (J4)

The M3A-HS11 includes the power supply connector pin for the SH7211.

Figure 3.1.5 shows a pin assignment of power supply connector.

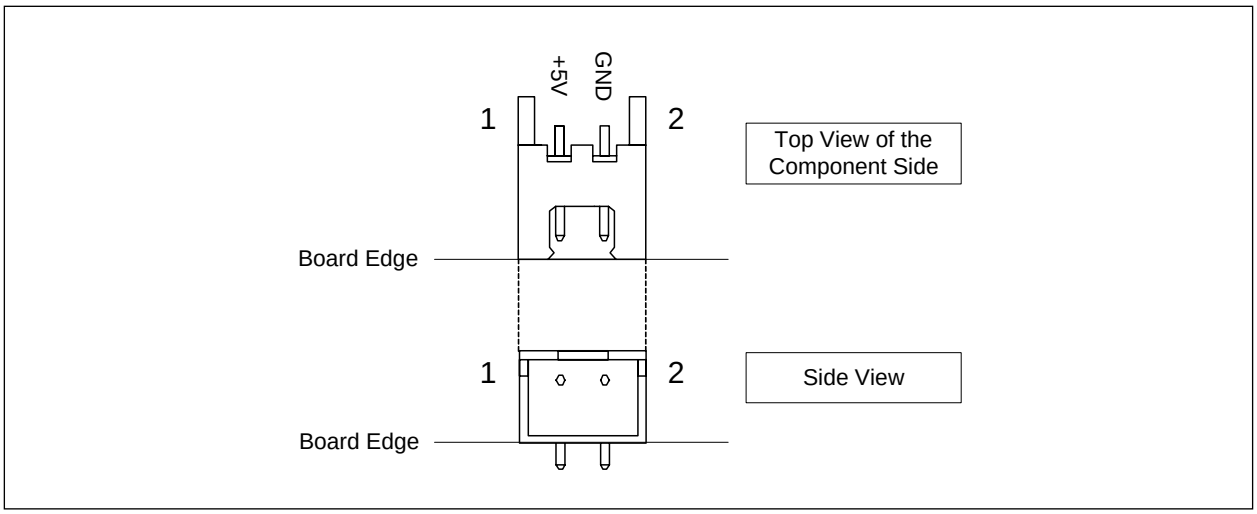


Figure 3.1.5 Pin Assignment of Power Supply Connector (J4)

Table 3.1.4 lists a pin assignment of power supply connector for M3A-HS11.

Table 3.1.4 Pin Assignment of Power Supply Connector (J4)

Pin	Signal Name	Pin	Signal Name
1	+ 5V	2	GND

3.1.4 External Power Supply Connector for SH7211 (J5, J6)

The M3A-HS11 includes the external power supply connector pins to supply the power source of 3.3V and 1.5V externally.

When the power is supplied by using this connector, set the power select jumper (JP1 and JP2) to “2-3”.

Figure 3.1.6 shows a pin assignment of power supply connector.

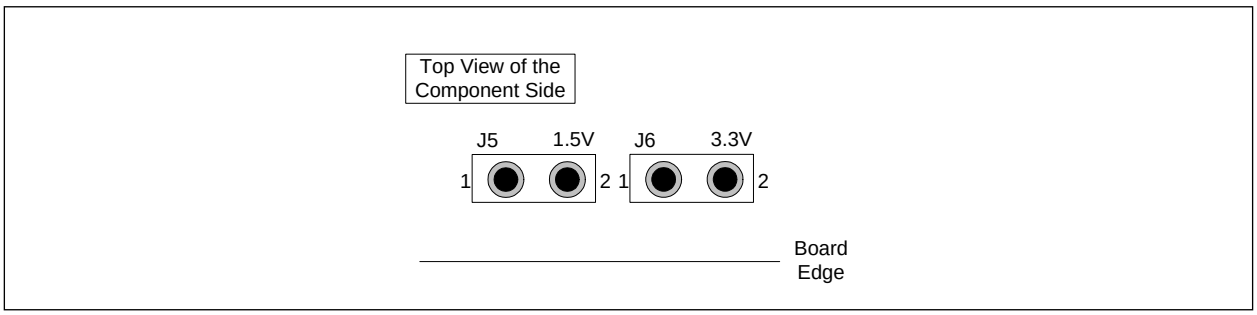


Figure 3.1.6 Pin Assignment of Power Supply Connector (J5, J6)

Table 3.1.5 lists a pin assignment of power supply connector (J5) for SH7211.

Table 3.1.5 Pin Assignment of Power Supply Connector (J5)

Pin	Signal Name	Pin	Signal Name
1	+5V	2	GND

Table 3.1.6 lists a pin assignment of power supply connector (J6) for SH7211.

Table 3.1.6 Pin Assignment of Power Supply Connector (J6)

Pin	Signal Name	Pin	Signal Name
1	+3.3V	2	GND

3.1.5 A/D, D/A Connector (J7)

The M3A-HS11 includes the A/D and D/A connector pins which the A/D and D/A pins of SH7211 are connected. When the voltages of AVCC and AVREF are supplied through this connector, remove the AVCC select jumper (JP3) and AVREF select jumper (JP4). Figure3.1.7 shows a pin assignment of A/D and D/A connectors. Table3.1.7 lists pin assignments of A/D and D/A connector (J7).

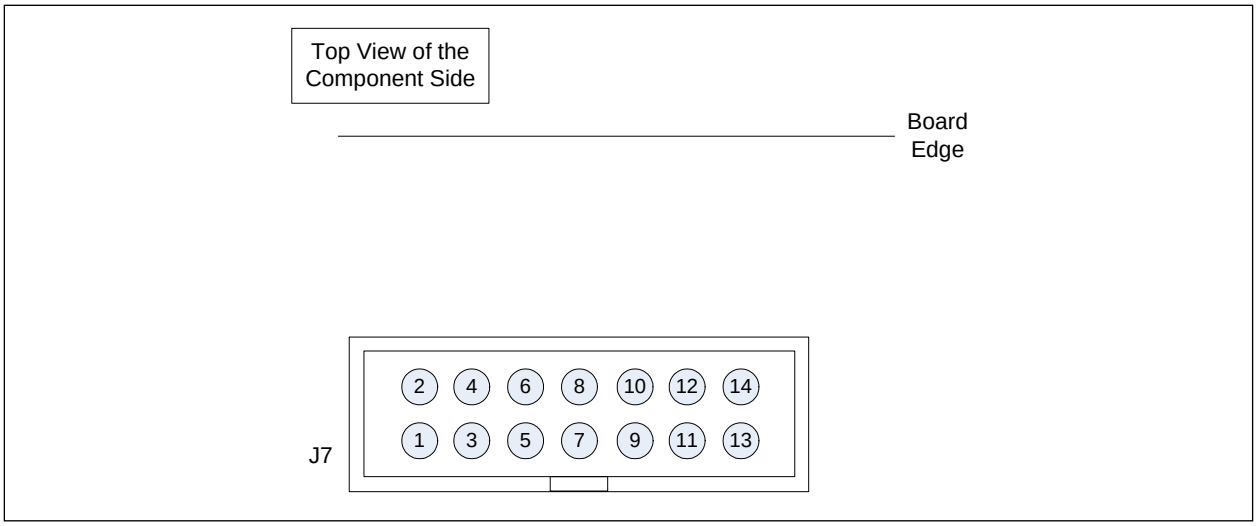


Figure3.1.7 Pin Assignment of A/D and D/A connector

Table3.1.7 Pin Assignments of A/D and D/A connector (J7)

Pin	Signal Name
1	AVCC
2	GND
3	AVREF
4	GND
5	AN7
6	AN6
7	AN5
8	AN4
9	AN3
10	AN2
11	AN1
12	AN0
13	DA0
14	DA1

3.1.6 Extension Connectors (J8-J12)

The M3A-HS11 includes the through hole for mounting extension connectors to which the I/O pins of the SH7211 are connected.

MIL standard connectors can be connected to J8-J12, allowing the user to connect with extension boards or monitor the SH7211 bus signals.

The address signal of SH7211 is connected to the terminal J9 connector through J8 connector. Moreover, the bus signal of SH7211 is connected to the terminal J12 connector through J11 connector. J8 connector and J11 connector are mounted for signal measurement by measuring instrument. When an extension board is made, it is recommended to use the J9 and J12 of terminal connector to prevent the waveform distortion occurred by the reflection of signal.

Figure3.1.8 shows a pin assignment of extension connector.

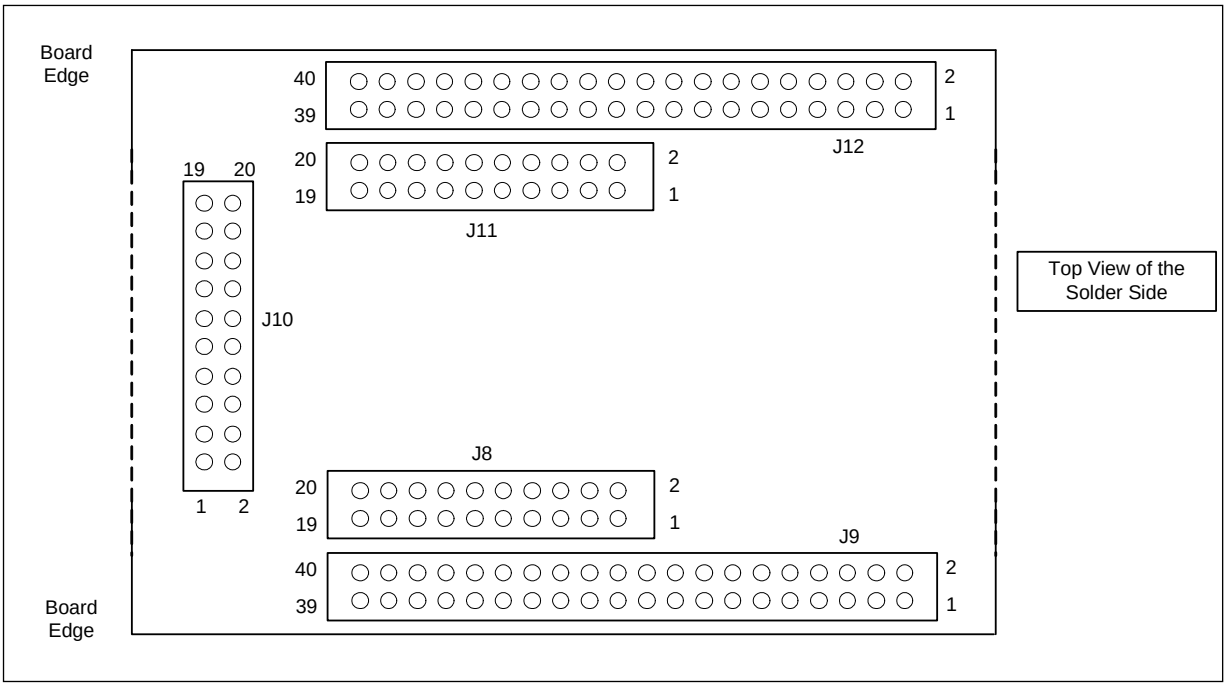


Figure3.1.8 Pin Assignment of Extension Connectors

Table3.1.8 lists pin assignments of extension connector (J8).

Table3.1.8 Pin Assignments of Extension Connectors (J8)

Pin	Signal Name	Other Connection
1	NC	-
2	NC	-
3	EXCLK(PB3/CKIO)	Clock Buffer(Not mounted), SDRAM, Extension Connector (J9)
4	PA9/A9	SDRAM, SRAM, Extension Connector (J9)
5	PA8/A8	SDRAM, SRAM, Extension Connector (J9)
6	PA7/A7	SDRAM, SRAM, Extension Connector (J9)
7	PA6/A6	SDRAM, SRAM, Extension Connector (J9)
8	PA5/A5	SDRAM, SRAM, Extension Connector (J9)
9	PA4/A4	SDRAM, SRAM, Extension Connector (J9)
10	PA3/A3	SDRAM, SRAM, Extension Connector (J9)
11	PA2/A2	SDRAM, SRAM, Extension Connector (J9)
12	PA1/A1	SDRAM, SRAM, Extension Connector (J9)
13	PA0/A0	Extension Connector (J9)
14	PB2/SCK0/$\overline{\text{POE4}}$/$\overline{\text{CS0}}$	Extension Connector (J9, J12)
15	PB16/TXD0/$\overline{\text{POE1}}$/$\overline{\text{CS1}}$	Extension Connector (J9)
16	PB21/TIOC3BS/RXD0/IRQ0/$\overline{\text{CS2}}$	LED7, Extension Connector (J9)
17	PB18/TIOC3B/IRQ4/$\overline{\text{CS4}}$	SRAM, Extension Connector (J9)
18	PB15/TIOC3C/IRQ5/$\overline{\text{CS5}}$	DIP Switch for User (SW3-1), Extension Connector (J9, J12)
19	$\overline{\text{RESET}}$	Reset Module, H-UDI Connector (J1, J2), Extension Connector (J9)
20	GND	-

Table3.1.9 lists pin assignments of extension connectors (J9).

Table3.1.9 Pin Assignments of Extension Connectors (J9)

Pin	Signal Name	Other Connection
1	3.3V	-
2	3.3V	-
3	$\overline{\text{WDTOVF}}$	-
4	PA25/TXD1/TIOC0D/IRQ7/A25	Serial Port Connector (J3)
5	PA24/RXD1/TIOC0C/IRQ6/A24	Serial Port Connector (J3)
6	PA23/SCK1/TIOC0B/IRQ5/A23	Extension Connector (J12)
7	PA22/TIOC0A/IRQ4/A22	Extension Connector (J10)
8	PA21/IRQ3/A21	IRQ3 Switch (SW6)
9	PA20/IRQ2/A20	SRAM
10	PA19/IRQ1/A19	SRAM
11	PA18/IRQ0/A18	SRAM
12	PA17/TXD3/A17	SRAM
13	PA16/RXD3/A16	SRAM
14	PA15/SCK3/A15	SRAM
15	PA14/A14	SDRAM, SRAM
16	PA13/A13	SDRAM, SRAM
17	PA12/A12	SDRAM, SRAM
18	PA11/A11	SDRAM, SRAM
19	PA10/A10	SDRAM, SRAM
20	GND	-
21	NC	-
22	NC	-
23	EXCLK	Clock Buffer (Not mounted), SDRAM, Extension Connector (J8)
24	PA9/A9	SDRAM, SRAM, Extension Connector (J8)
25	PA8/A8	SDRAM, SRAM, Extension Connector (J8)
26	PA7/A7	SDRAM, SRAM, Extension Connector (J8)
27	PA6/A6	SDRAM, SRAM, Extension Connector (J8)
28	PA5/A5	SDRAM, SRAM, Extension Connector (J8)
29	PA4/A4	SDRAM, SRAM, Extension Connector (J8)
30	PA3/A3	SDRAM, SRAM, Extension Connector (J8)
31	PA2/A2	SDRAM, SRAM, Extension Connector (J8)
32	PA1/A1	SDRAM, SRAM, Extension Connector (J8)
33	PA0/A0	Extension Connector (J8)
34	PB2/SCK0/$\overline{\text{POE4}}$/$\overline{\text{CS0}}$	Extension Connector (J8, J12)
35	PB16/TXD0/$\overline{\text{POE1}}$/$\overline{\text{CS1}}$	Extension Connector (J8)
36	PB21/TIOC3BS/RXD0/IRQ0/$\overline{\text{CS2}}$	LED7, Extension Connector (J8)
37	PB18/TIOC3B/IRQ4/$\overline{\text{CS4}}$	SRAM, Extension Connector (J8)
38	PB15/TIOC3C/IRQ5/$\overline{\text{CS5}}$	DIP Switch for User (SW3-1), Extension Connector (J8, J12)
39	$\overline{\text{RESET}}$	Reset Module, H-UDI Connector (J1, J2), Extension Connector (J8)
40	GND	-

Table3.1.10 lists pin assignments of extension connectors.

Table3.1.10 Pin Assignments of Extension Connectors (J10)

Pin	Signal Name	Other connection
1	PF1/SDA/$\overline{\text{POE3}}$/IRQ1	EEPROM
2	PF0/SCL/$\overline{\text{POE7}}$/IRQ0	EEPROM
3	PB17/TIOC3A/IRQ1/$\overline{\text{CS3}}$	SDRAM
4	PB1/TXD0/$\overline{\text{POE8}}$/RD/$\overline{\text{WR}}$	SDRAM, SRAM
5	PB8/RXD3/TIOC3AS/$\overline{\text{WE0}}$/$\overline{\text{DQMLL}}$	SDRAM, SRAM
6	PB9/TXD3/TIOC3CS/$\overline{\text{WE1}}$/$\overline{\text{WE}}$/$\overline{\text{DQMLU}}$	SDRAM, SRAM
7	NC	-
8	NC	-
9	PB4/TIOC4A/CKE	SDRAM
10	PB5/TIOC4B/IRQ2/$\overline{\text{RASL}}$	SDRAM
11	PB6/TIOC4C/IRQ3/$\overline{\text{CASL}}$	SDRAM
12	PB7/TIOC4D/IRQ7/$\overline{\text{CS7}}$	Extension Connector (J12)
13	PB13/SCK2/TIOC4BS/$\overline{\text{BACK}}$	LED5, Extension Connector (J12)
14	PB11/TXD2/TIOC4DS/$\overline{\text{AH}}$/DACK3	LED3
15	PB10/RXD2/TIOC4CS/$\overline{\text{WAIT}}$/DREQ3	LED2, Extension Connector (J12)
16	NC	-
17	PA22/TIOC0A/IRQ4/A22	Extension Connector (J9)
18	PB12/TXD2/TIOC4AS/$\overline{\text{BREQ}}$	LED4, Extension Connector (J12)
19	PB19/TIOC3D/IRQ6/$\overline{\text{CS6}}$	DIP Switch for User (SW3-2)
20	GND	-

Table3.1.11 lists pin assignments of extension connectors (J11).

Table3.1.11 Pin Assignments of Extension Connectors (J11)

Pin	Signal Name	Other Connection
1	NC	-
2	NC	-
3	PB0/RXD0/$\overline{\text{POE0}}$/$\overline{\text{RD}}$	SRAM, Extension Connector (J12)
4	PD15/D15/TIC5US	SDRAM, SRAM, Extension Connector (J12)
5	PD14/D14/TIC5VS	SDRAM, SRAM, Extension Connector (J12)
6	PD13/D13/TIC5WS	SDRAM, SRAM, Extension Connector (J12)
7	PD12/D12/TIC5U	SDRAM, SRAM, Extension Connector (J12)
8	PD11/D11/TIC5V	SDRAM, SRAM, Extension Connector (J12)
9	PD10/D10/TIC5W	SDRAM, SRAM, Extension Connector (J12)
10	PD9/D9	SDRAM, SRAM, Extension Connector (J12)
11	PD8/D8	SDRAM, SRAM, Extension Connector (J12)
12	PD7/D7	SDRAM, SRAM, Extension Connector (J12)
13	PD6/D6	SDRAM, SRAM, Extension Connector (J12)
14	PD5/D5	SDRAM, SRAM, Extension Connector (J12)
15	PD4/D4	SDRAM, SRAM, Extension Connector (J12)
16	PD3/D3	SDRAM, SRAM, Extension Connector (J12)
17	PD2/D2	SDRAM, SRAM, Extension Connector (J12)
18	PD1/D1	SDRAM, SRAM, Extension Connector (J12)
19	PD0/D0	SDRAM, SRAM, Extension Connector (J12)
20	GND	-

Table3.1.12 lists pin assignments of the extension connectors (J12).

Table3.1.12 Pin Assignments of the Extension Connectors (J12)

Pin	Signal Name	Other connection
1	+5V	-
2	+5V	-
3	PB10/RXD2/TIOC4CS/$\overline{\text{WAIT}}$/DREQ3	LED2, Extension Connector (J10)
4	PB15/TIOC3C/IRQ5/$\overline{\text{CS5}}$	DIP Switch for User (SW3-1) , Extension Connector (J8,J9)
5	PB14/RXD2/$\overline{\text{ADTRG}}$/$\overline{\text{MRES}}$	-
6	PB13/SCK2/TIOC4BS/$\overline{\text{BACK}}$	LED5, Extension Connector (J10)
7	PB12/TXD2/TIOC4AS/$\overline{\text{BREQ}}$	LED4, Extension Connector (J10)
8	PB28/RXD3/TIOC1A/DACK0	DIP Switch for User (SW3-3)
9	PB7/TIOC4D/IRQ7/$\overline{\text{CS7}}$	Extension Connector (J10)
10	PB29/TIOC1B/DREQ0	DIP Switch for User (SW3-4)
11	NC(When R106 is mounted, PB30/ $\overline{\text{ASEBRKAK}}$ / $\overline{\text{ASEBRK}}$ / $\overline{\text{UBCTRG}}$ / $\overline{\text{IRQOUT}}$)	- (H-UDI Connector (J1))
12	NC(When R107 is mounted, PB27/AUDATA0/TXD3/TIOC2A/TEND0)	- (H-UDI Connector (J1))
13	NC(When R108 is mounted, PB26/AUDATA1/SCK3/TIOC2B/DREQ1)	- (H-UDI Connector (J1))
14	NC(When R102 is mounted, PB25/AUDATA2/TXD3/TCLKA/IRQ3/DACK1)	- (H-UDI Connector (J1))
15	NC(When R109 is mounted, PB24/AUDATA3/RXD3/TCLKB/IRQ2/TEND1)	- (H-UDI Connector (J1))
16	NC(When R110 is mounted, PB23/AUDCK/TXD2/TCLKC/DREQ2)	- (H-UDI Connector (J1))
17	NC(When R111 is mounted, PB22/ $\overline{\text{AUDSYNC}}$ /RXD2/TCLKD/DACK2/ $\overline{\text{FRAME}}$)	- (H-UDI Connector (J1))
18	NC	-
19	PB20/TIOC3DS/$\overline{\text{BS}}$	LED6
20	GND	-
21	PA23/SCK1/TIOC0B/IRQ5/A23	Extension Connector (J9)
22	PB2/SCK0/$\overline{\text{POE4}}$/$\overline{\text{CS0}}$	Extension Connector (J8,J9)
23	PB0/RXD0/$\overline{\text{POE0}}$/$\overline{\text{RD}}$	SRAM, Extension Connector (J11)
24	PD15/D15/TIC5US	SDRAM, SRAM, Extension Connector (J11)
25	PD14/D14/TIC5VS	SDRAM, SRAM, Extension Connector (J11)
26	PD13/D13/TIC5WS	SDRAM, SRAM, Extension Connector (J11)
27	PD12/D12/TIC5U	SDRAM, SRAM, Extension Connector (J11)
28	PD11/D11/TIC5V	SDRAM, SRAM, Extension Connector (J11)
29	PD10/D10/TIC5W	SDRAM, SRAM, Extension Connector (J11)
30	PD9/D9	SDRAM, SRAM, Extension Connector (J11)
31	PD8/D8	SDRAM, SRAM, Extension Connector (J11)
32	PD7/D7	SDRAM, SRAM, Extension Connector (J11)
33	PD6/D6	SDRAM, SRAM, Extension Connector (J11)
34	PD5/D5	SDRAM, SRAM, Extension Connector (J11)
35	PD4/D4	SDRAM, SRAM, Extension Connector (J11)
36	PD3/D3	SDRAM, SRAM, Extension Connector (J11)
37	PD2/D2	SDRAM, SRAM, Extension Connector (J11)
38	PD1/D1	SDRAM, SRAM, Extension Connector (J11)
39	PD0/D0	SDRAM, SRAM, Extension Connector (J11)
40	GND	-

3.2 Outline of Switches and LEDs

The M3A-HS11 includes switches and LEDs as its operational components.

Figure3.2.1 shows the M3A-HS11 operational component assignment.

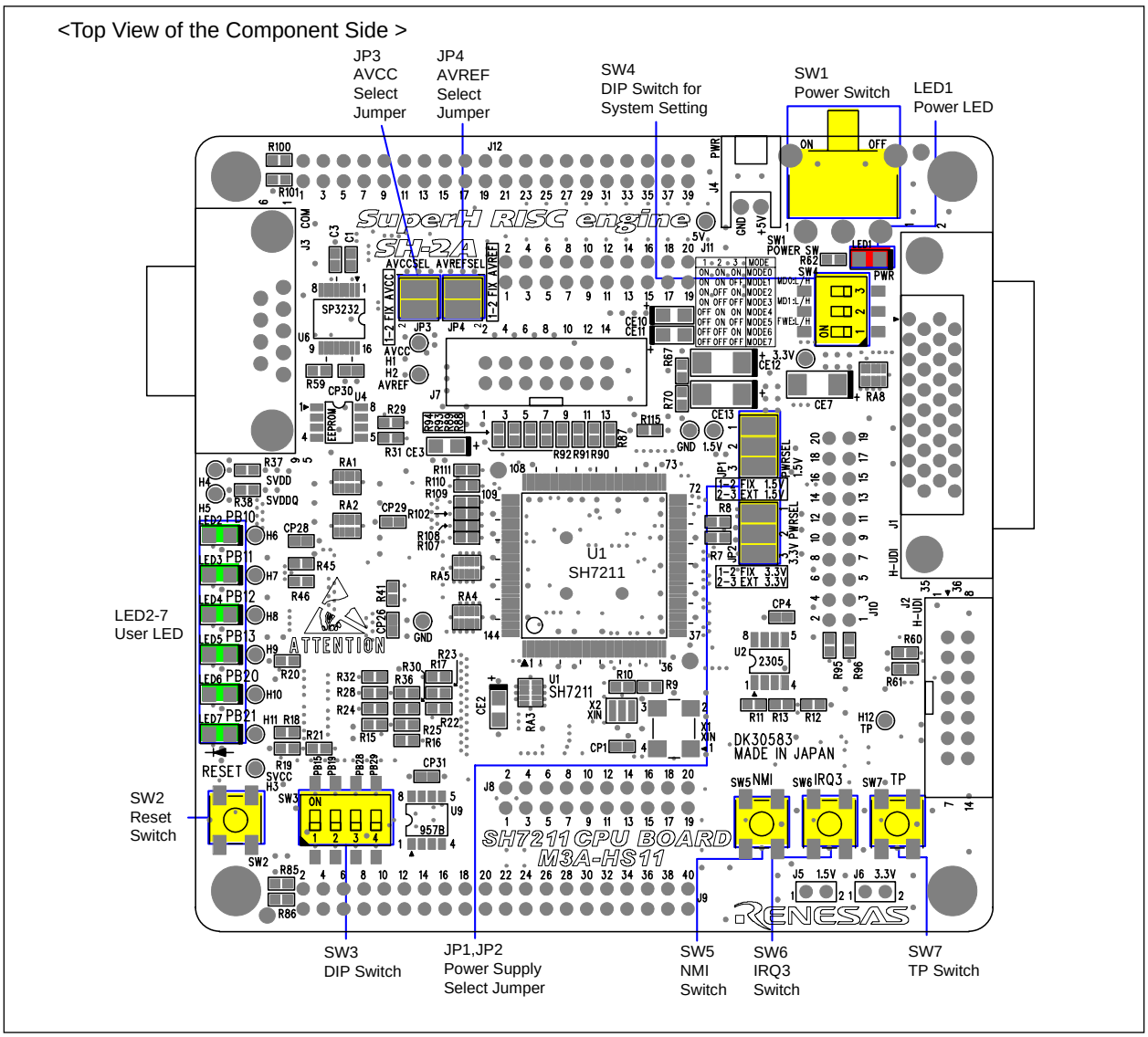


Figure3.2.1 M3A-HS11 Operational Component Assignment

3.2.1 SH7211 Power Supply Select Jumpers (JP1, JP2)

The sources for the SH7211 power supply voltages can be selected by setting JP1 and JP2.

Figure 3.2.2 shows the SH7211 power supply voltage select jumper assignment and Table 3.2.1 lists the jumper setting for selecting SH7211 power supply.

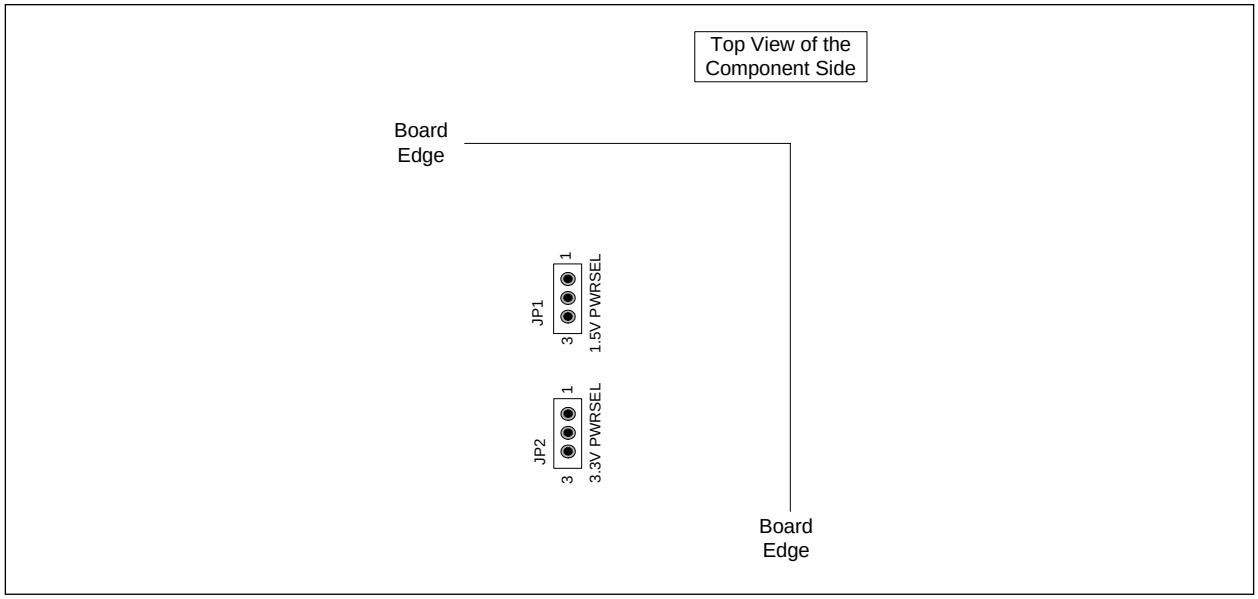


Figure 3.2.2 SH7211 Power Supply Select Jumper Assignment (JP1, JP2)

Table 3.2.1 Jumper Setting for Power Supply Select (JP1, JP2)

Jumper	Setting	Function
JP1 1.5V PWRSEL	1 - 2	1.5V fixed power supply voltage (supplied from regulator)
	2 - 3	External power supply voltage (supplied from J5)
JP2 3.3V PWRSEL	1 - 2	3.3V fixed power supply voltage (supplied from regulator)
	2 - 3	External power supply voltage (supplied from J6)

: Initial Setting

Note: Do not change jumper settings during the operation of M3A-HS11. Ensure to turn off the power for the M3A-HS11 before changing jumper settings.

3.2.2 AVCC and AVREF Select Jumper (JP3, JP4)

The sources for the SH7211 power supply voltages supplied to AVCC and AVREF can be selected by setting JP3 and JP4.

Figure3.2.3 shows the pin assignment of AVCC and AVREF select jumper. Table3.2.2 lists the jumper setting of AVCC and AVREF select jumper.

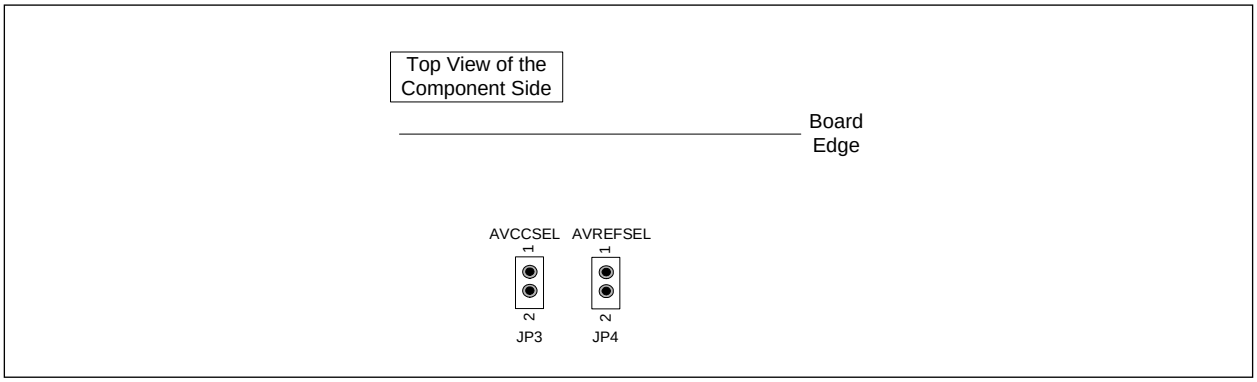


Figure3.2.3 Pin Assignment of AVCC and AVREF Select Jumper (JP3, JP4)

Table3.2.2 Jumper Setting of AVCC and AVREF Select Jumper (JP3, JP4)

Jumper	Setting	Function
JP3 AVCCSEL	1 - 2	AVCC of SH7211 is connected with 5V fixed power supply voltage
	Open	External Power Supply Voltage (supplied from J7 or H1)
JP4 AVREFSEL	1 - 2	AVREF of SH7211 is connected with 5V fixed power supply voltage
	Open	External Power Supply Voltage (supplied from J7 or H2)

: Initial Setting

Note: Do not change jumper settings during the operation of M3A-HS11. Ensure to turn off the power for the M3A-HS11 before changing jumper settings.

3.2.3 Switch and LED Functions

The M3A-HS11 includes seven switches and seven LEDs.

Table3.2.3 lists switches mounted on M3A-HS11.

Table3.2.3 Switches Mounted on M3A-HS11

No.	Function	Remarks
SW1	System Power On/Off Switch	-
SW2	System Reset Input Switch	See Section 2.8 for details
SW3	DIP Switch for User (4-pole) SW3-1 OFF : PB15=H, ON : PB15=L SW3-2 OFF : PB19=H, ON : PB19=L SW3-3 OFF : PB28=H, ON : PB28=L SW3-4 OFF : PB29=H, ON : PB29=L	*PB15, PB19, PB28 and PB29 are pulled up. See section 2.5 2 for details.
SW4	DIP Switch for System Setting (4-pole)	See Table3.2.4 for the functions
SW5	NMI Switch	See Section 2.9 for details
SW6	IRQ3 Switch	See Section 2.9 for details
SW7	TR Switch	See Section 2.9 for details

Table3.2.4 lists the functions of switch SW4. SH7211 operating mode is set by the combination of the MD0, MD1 and FWE pins. Table3.2.5 lists the setting of SH7211 operating modes.

Table3.2.4 Functions of Switch SW4

No.	Setting	Function	
SW4-1 FWE	OFF	FWE=H (Releasing the writing/erasing protects of on-chip flash memory)	MCU operating mode setting (See.Table3.2.5)
	ON	FWE=L (Setting the writing/erasing protects of on-chip flash memory)	
SW4-2 MD1	OFF	MD1 pin state “H”	
	ON	MD1 pin state “L”	
SW4-3 MD0	OFF	MD0 pin state “H”	
	ON	MD0 pin state “L”	

: Initial Setting

Table3.2.5 Selection of SH7211 Operating Modes

SW4-1 (FWE)	SW4-2 (MD1)	SW4-3 (MD0)	SH7211 Operating Mode	
			Operating mode	Mode name
ON	ON	ON	Mode0	MCU extension mode0 (On-chip ROM disabled, CSO space:16bit bus)
ON	ON	OFF	Mode1	MCU extension mode1 (On-chip ROM disabled, CSO space:8bit bus))
ON	OFF	ON	Mode2	MCU extension mode2 (On-chip ROM enabled)
ON	OFF	OFF	Mode3	Single chip mode (On-chip ROM enabled)
OFF	ON	ON	Mode4	Boot mode (On-chip ROM enabled)
OFF	ON	OFF	Mode5	User boot mode (On-chip ROM enabled)
OFF	OFF	ON	Mode6	User programming mode (On-chip ROM enabled)
OFF	OFF	OFF	Mode7	Writer mode (On-chip ROM enabled)

: Initial Setting

Table3.2.6 lists the functions of LEDs mounted in M3A-HS11.

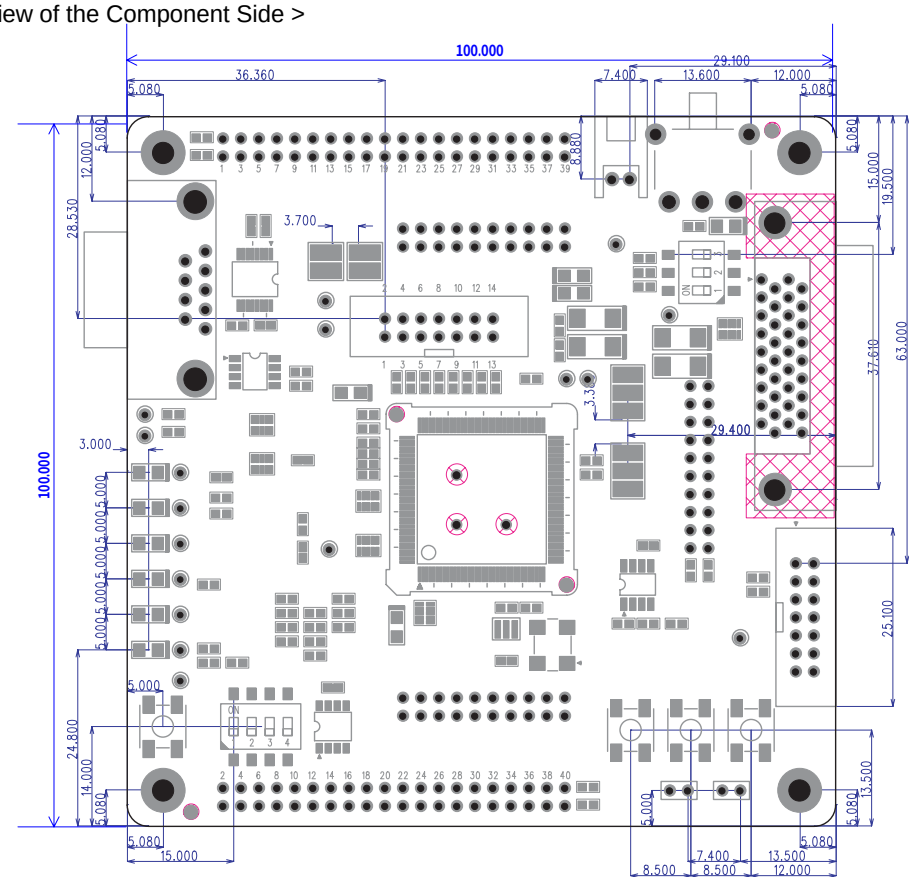
Table3.2.6 Functions of LEDs mounted in M3A-HS11

No.	Color	Functions/Remarks
LED1	Red	Power-on LED (LED1 lights when power is supplied)
LED2	Green	Open to users (LED2 lights when PB10 outputs “L”)
LED3	Green	Open to users (LED3 lights when PB11 outputs “L”)
LED4	Green	Open to users (LED4 lights when PB12 outputs “L”)
LED5	Green	Open to users (LED5 lights when PB13 outputs “L”)
LED6	Green	Open to users (LED6 lights when PB20 outputs “L”)
LED7	Green	Open to users (LED7 lights when PB21 outputs “L”)

3.3 Board Dimensions of M3A-HS11

Figure 3.3.1 shows board dimensions of M3A-HS11.

<Top View of the Component Side >



< Top View of the Solder Side >

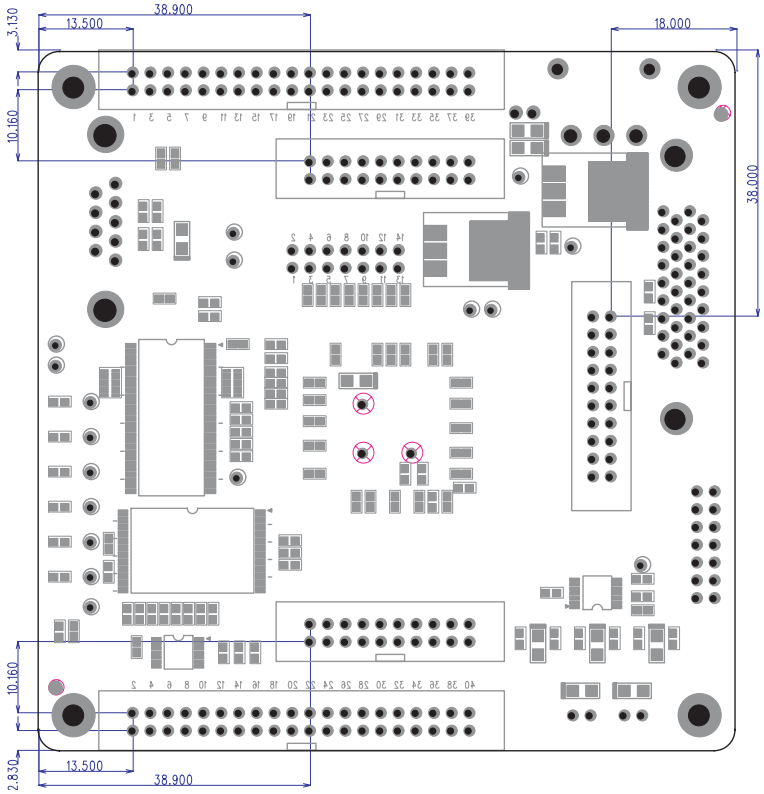


Figure 3.3.1 Board Dimensions of M3A-HS11

Appendix

M3A-HS11 SCHEMATICS

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SH7211 CPU BOARD M3A-HS11 SCHEMATICS

TITLE	PAGE
INDEX	1
CPU SH7211/SRAM/SDRAM/EEPROM	2
UDI/RESET/UART/POWER	3
BUS CONNECTORS/PUSH SW	4

Note:

5VCC = 5V
3VCC = 3.3V
1.5VCC = 1.5V

R = Fixed Resistors
RA = Resistor Array
C = Ceramic Caps
CE = Tantalum Electrolytic Caps
CP = Decoupling Caps

[ ] :not mounted

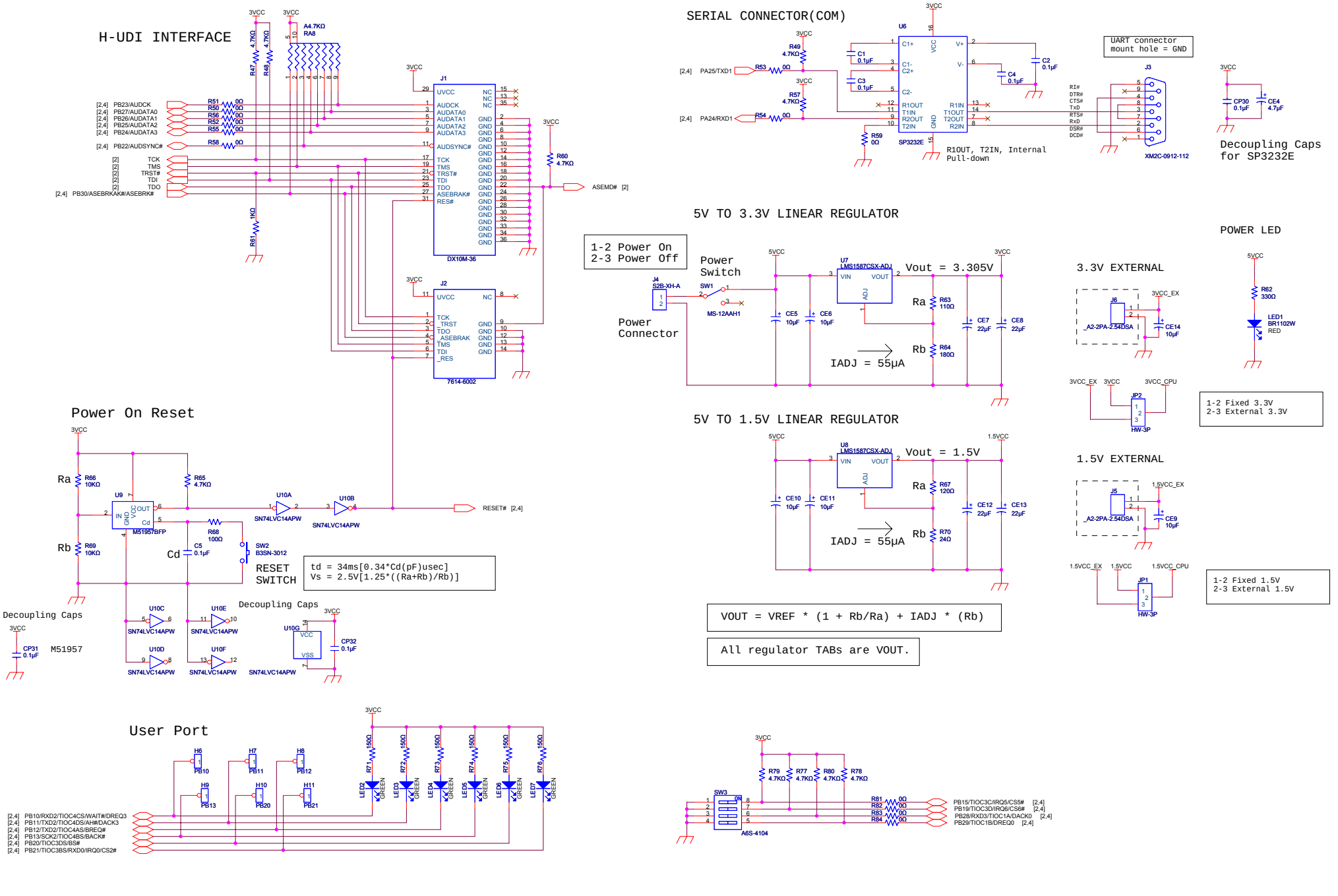
CHANGE				RENESAS SOLUTIONS CORPORATION				M3A-HS11
		SCALE		DRAWN	CHECKED	DESIGNED	APPROVED	INDEX (1 / 4)
Ver. 1.01		DATE	07-12-18					DK30583

Clock Mode : Mode6 Only
Operating Mode :

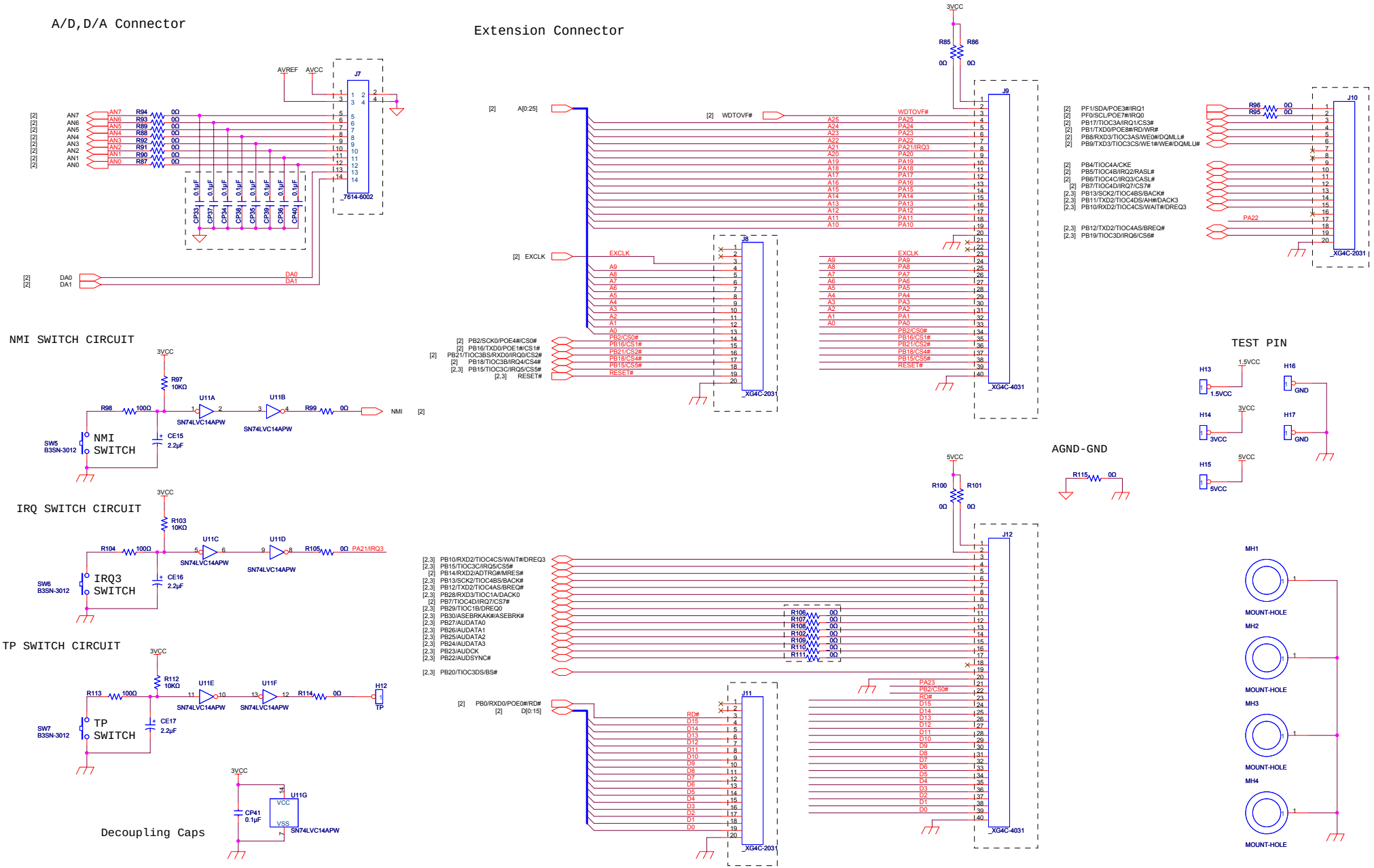
1	2	3	Mode
ON	ON	ON	MODE0;MCU extension mode 0
		OFF	MODE1;MCU extension mode 1
	OFF	ON	MODE2;MCU extension mode 2
		OFF	MODE3;Single chip mode
OFF	ON	ON	MODE4;Boot mode
		OFF	MODE5;User Boot mode
	OFF	ON	Mode6;User Programming mode
		OFF	Mode7;Writer mode

10.00MHz
SH7211 Bus Connector Clock
10.00MHz CERALOCK
SG8002CA_10.00MHz
CSTCE-G10M0
CY2305SC-1H
SRAM
SRAM CS AREA4
16bit access = 2MB
Decoupling Caps
R1LV1616RSA-7S
EEPROM
HN58X24128FPIE
SDRAM
SDRAM CS AREA3
16bit access = 16MB
DUMPING REGISTER for SDRAM
EDS1216AATA
Mode Switch
A6S-3101
SH7211
1-2 FIX AVCC
1-2 FIX AVREF
Decoupling Caps

CHANGE		SCALE		RENESAS SOLUTIONS CORPORATION				M3A-HS11
				DRAWN	CHECKED	DESIGNED	APPROVED	CPU SH7211,SRAM,SDRAM,EEPROM (2 / 4)
Ver. 1.01		DATE	07-12-18					DK30583



CHANGE		SCALE		RENESAS SOLUTIONS CORPORATION	M3A-HS11
Ver. 1.01		DATE	07-12-18	DRAWN / CHECKED / DESIGNED / APPROVED	H-UDI/RESET/UART/POWER (3 / 4)
					DK30583



CHANGE			RENESAS SOLUTIONS CORPORATION		M3A-HS11
			DRAWN / CHECKED / DESIGNED / APPROVED		BUS CONNECTORS/PUSH SW (4 / 4)
Ver. 1.01		SCALE			DK30583
		DATE	07-12-18		

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Revision History	SH7211 CPU Board M3A-HS11User's Manual

Rev.	Date of Issue	Content of Revision	
		Page	Page
1.00	Sep. 10, 2007	-	First edition issued.
1.01	Jan. 31, 2008	-	Errors corrected.

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M3A-HS11
User's Manual

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M3A-HS11
User's Manual

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